High Convergence: Low Cost Multi-Die Packaging Enables Pace Setting Performance

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August 27, 2012
Server Memory Challenges

- High capacity needed
- High performance in a multi-drop bus
- Signal quality to reduce soft bit errors
- Good signal amplitude
- Maintaining reference planes
- Good power delivery
Typical Server Class Memory Design

- Memory Controller
- Four channels
- 3 slots per channel
- RDIMM
Registered DIMM Architecture

Address and control: one load per slot

Data: one to four loads per slot
Zooming in on Signal Topologies

Typical 3 DIMM per channel (3DPC)

Each DRAM includes on-die termination to VTT
Zooming in on Signal Topologies

Registered Address Topology

Typical two rank design

External resistor termination to VTT
## Some Factors for Signal Quality

<table>
<thead>
<tr>
<th>Set by Application</th>
<th>Controllable</th>
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<tbody>
<tr>
<td>Frequency</td>
<td>Load matching</td>
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<tr>
<td>Switching time</td>
<td>Stub length</td>
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<tr>
<td>Total loading</td>
<td>Total parasitics</td>
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<td></td>
<td>Reference planes</td>
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<td>Power delivery</td>
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Standard Mono DRAM Packaging

Data signals
Address/control signals
Clocks
Gold wire bonds

Designed around needs of monolithic DRAM
Double Sided Boards

The “Bowtie” problem

Matching address signals are diagonally opposed

Results in long stubs
Bowtie Impact on Layout

Two routing layers just for bowtie

More crowded if stub length matching is done

Signal quality issues if stub length matching is not done
Standard Dual Die Packages

Same ballout as mono DRAM

Upper die far removed from signals due to long routing & wires

Symmetry between die may be compromised

Poor power delivery
Taming the Performance Beast

- Reduce overall parasitics
- Maintain reference plane
- Improve power delivery
- Shorten the stubs
Invensas Dual Face Down DRAM

Matched parasitics between DRAMs
(wirebond length difference = 0.1mm, compensated in substrate routing)

Reference planes maintained ball to die

Excellent power delivery
DFD Ballout Improvements

- Data signals
- Address/control signals
- Clocks
- Gold wire bonds

Package size = 11.5 x 11.5 mm
Multi-layer substrate ensures that data is referenced to VSS, address to VDD

Motherboards, DIMMs also follow this so return path is maintained silicon to silicon
Impact of DFD to Layout

70% reduction in stub length

“Bowtie” done in one routing layer
Full-DIMM Routing Comparison
Are We Out of Tricks?

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<table>
<thead>
<tr>
<th>PCB</th>
<th>Ball</th>
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<tbody>
<tr>
<td></td>
<td>Fat trace</td>
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<td></td>
<td>Power/ground</td>
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<td>Via</td>
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</table>

- DRAM
- Via in Pad

PCB

```
Layout with Via-in-Pad

- Improved power delivery
- Reduced inductance
- More copper flooding for thermal distribution
Example Design: 4Rx4 RDIMM

Simple 10 layer design

72 DRAM die
Signal Quality & Frequency

**Invensas @ 2133**
- Window = 798 ps
- Ideal tCK = 938 ps
- 85% of a tCK

**JEDEC card D @ 1333**
- Window = 1093 ps
- Ideal tCK = 1500 ps
- 73% of a tCK
Reality Check

2 DIMMs per channel

Running at DDR3-1600
Conclusions

High speed design limited by “death by a thousand paper cuts”

Using the monolithic ballout for DDPs introduces a lot of paper cuts

Rethinking DRAM stacking leads to new levels of module performance

Signal quality & power delivery can be significantly improved
Thank You

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