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High Convergence:

Low Cost Multi-Die Packaging

Enables Pace Setting

Performance

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Discobolus Designs

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Server Memory Challenges

High capacity needed

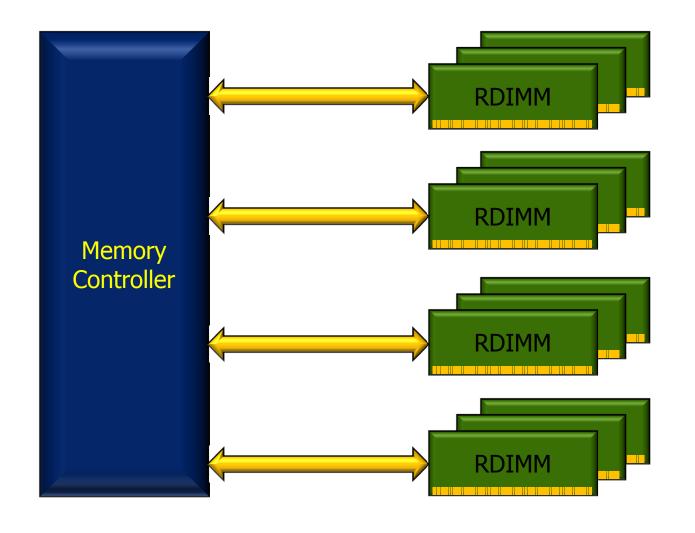High performance in a multi-drop bus

Signal quality to reduce soft bit errors

Good signal amplitude

Maintaining reference planes

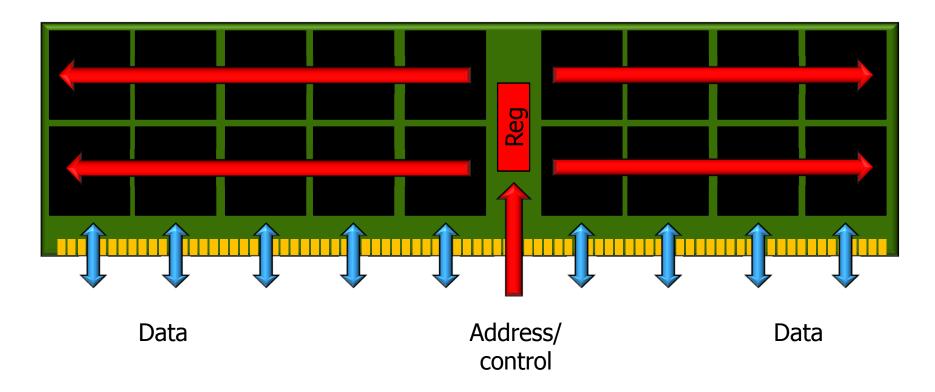Good power delivery

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Typical Server Class Memory Design
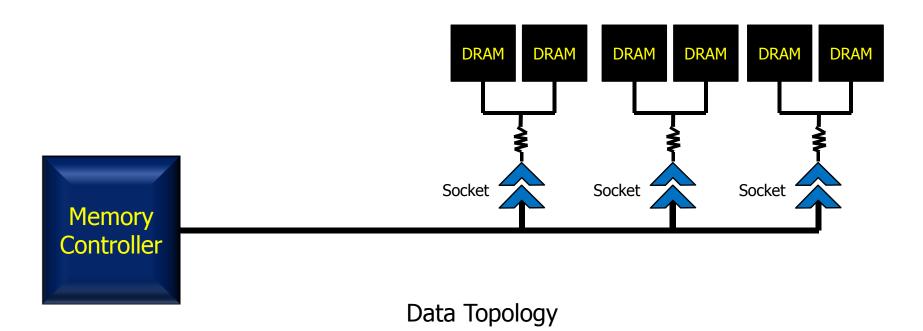

Four channels

3 slots per channel

Registered DIMM Architecture

Data

Address/
control

Data

Address and control: one load per slot

Data: one to four loads per slot

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Zooming in on Signal Topologies

DRAM DRAM   DRAM DRAM   DRAM DRAM

Socket   Socket   Socket
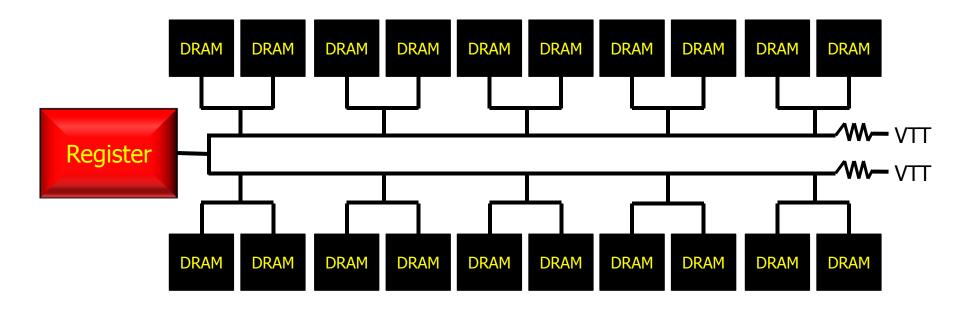
Memory
Controller

Data Topology

Typical 3 DIMM per channel (3DPC)

Each DRAM includes on-die termination to VTT

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Zooming in on Signal Topologies

Registered Address Topology

Typical two rank design

External resistor termination to VTT

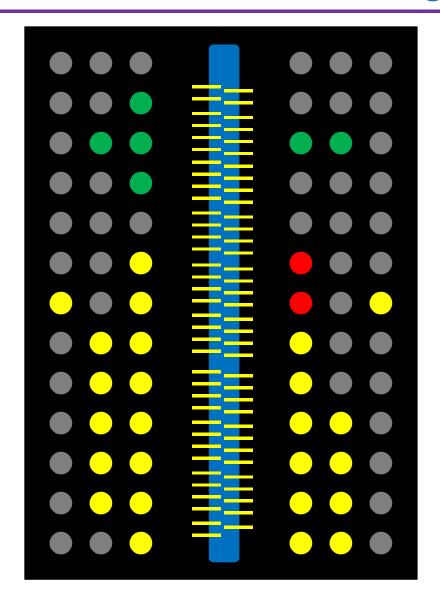## Some Factors for Signal Quality

Set by Application	Controllable
Frequency	Load matching
Switching time	Stub length
Total loading	Total parasitics
	Reference planes
	Power delivery

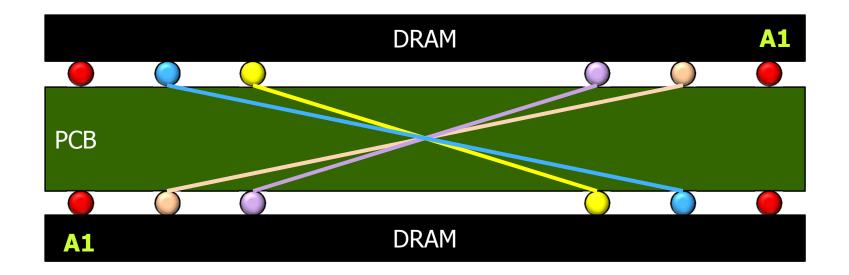invensas™

Standard Mono DRAM Packaging

Data signals

Address/control signals

Clocks

Gold wire bonds

Designed around needs
of monolithic DRAM

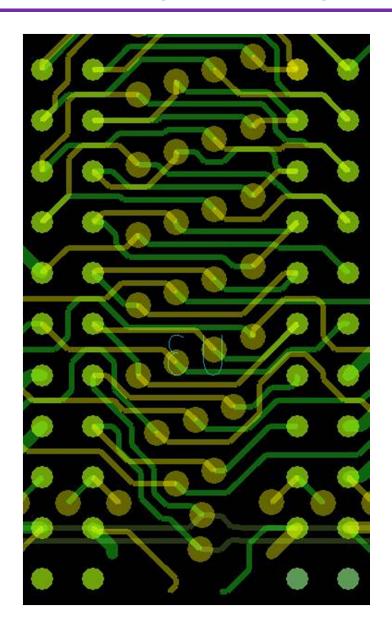invensas

Double Sided Boards

The "Bowtie" problem

Matching address signals
are diagonally opposed

Results in long stubs

Bowtie Impact on Layout

Two routing layers just for bowtie

More crowded if stub length matching is done

Signal quality issues if stub length matching is not done
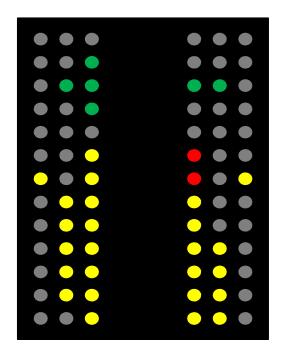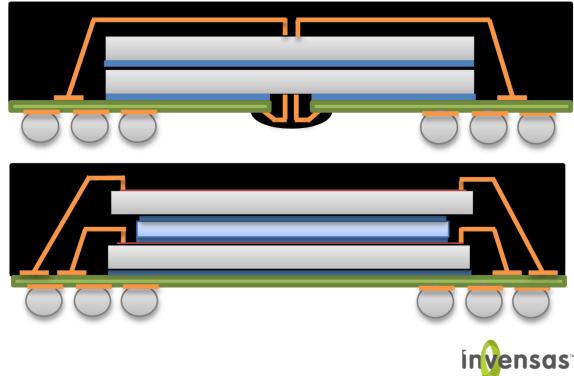
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Standard Dual Die Packages

Same ballout as mono DRAM

Upper die far removed from signals due to long routing & wires

Symmetry between die may be compromised

Poor power delivery

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Taming the Performance Beast

Reduce overall parasitics

Maintain reference plane

Improve power delivery

Shorten the stubs

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Invensas Dual Face Down DRAM

DRAM Die — Bond Wires — DRAM Die — Bond Wires — Spacer

Data — Address/control — Data
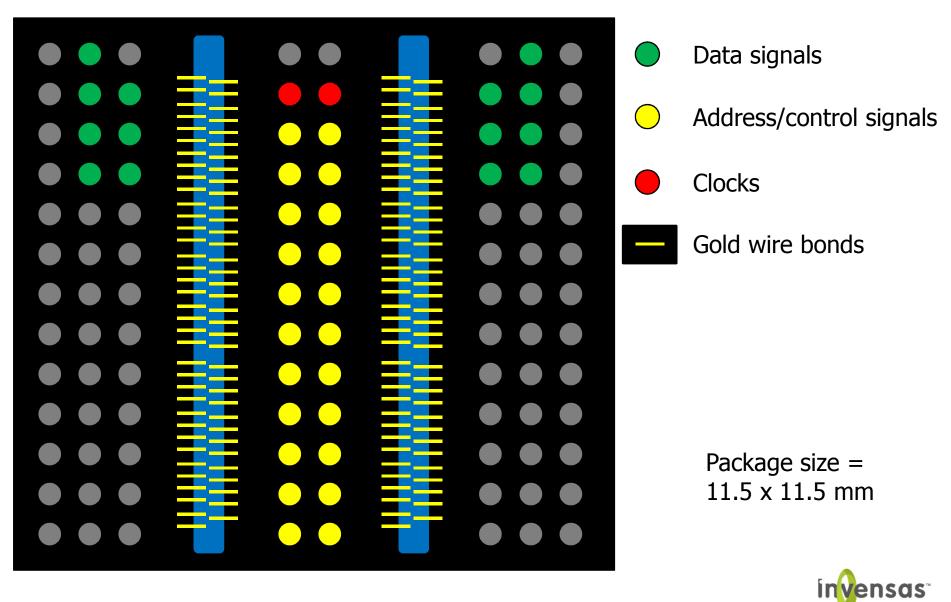
Matched parasitics between DRAMs
(wirebond length difference = 0.1mm,
compensated in substrate routing)

Reference planes maintained ball to die
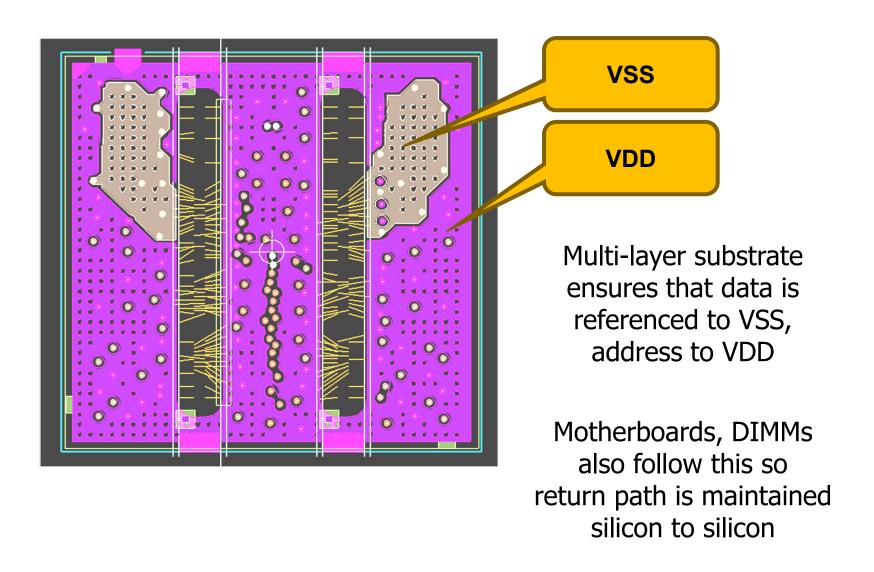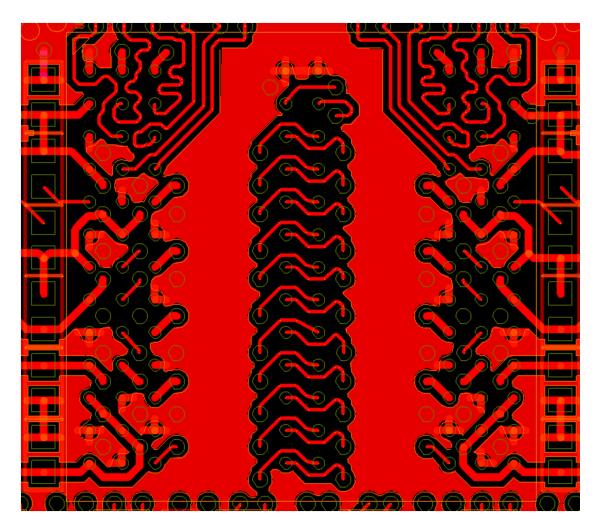
Excellent power delivery

DFD Ballout Improvements

- 🟢 Data signals
- 🟡 Address/control signals
- 🔴 Clocks
- ▬ Gold wire bonds

Package size = 11.5 x 11.5 mm

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Reference Planes

VSS

VDD

Multi-layer substrate ensures that data is referenced to VSS, address to VDD

Motherboards, DIMMs also follow this so return path is maintained silicon to silicon
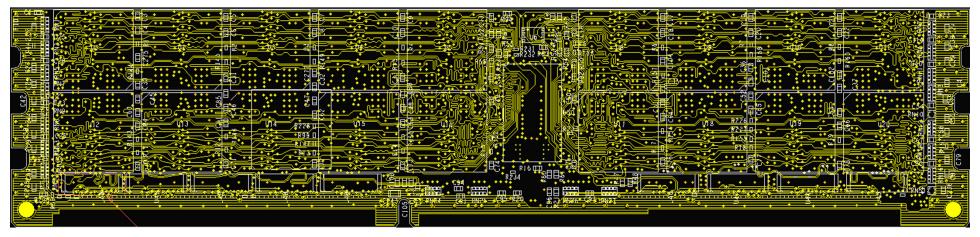
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Impact of DFD to Layout
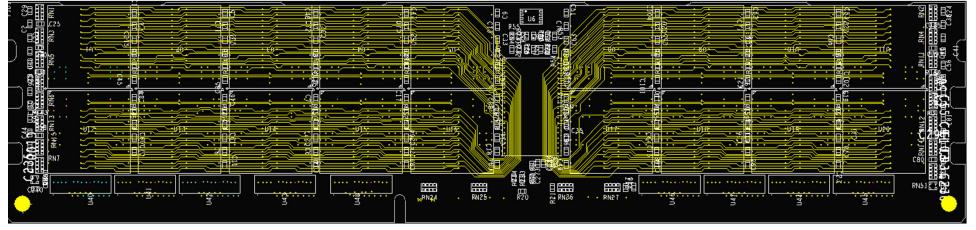

70% reduction in stub length

"Bowtie" done in one routing layer

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Full-DIMM Routing Comparison

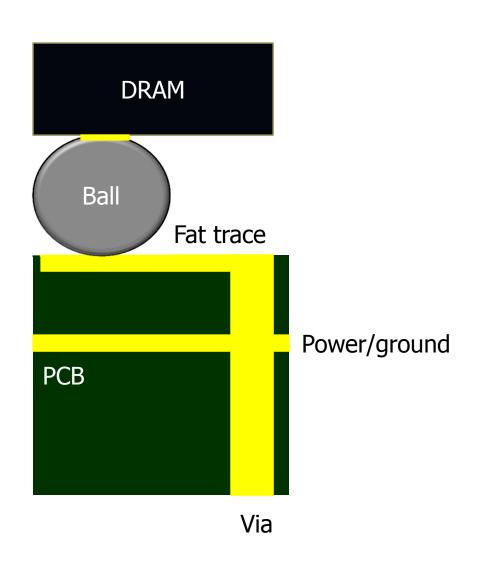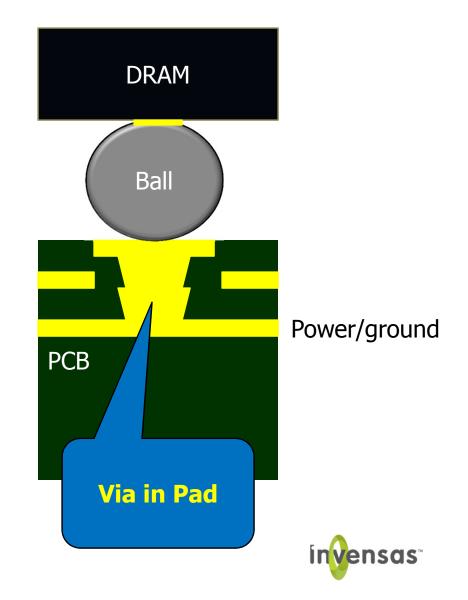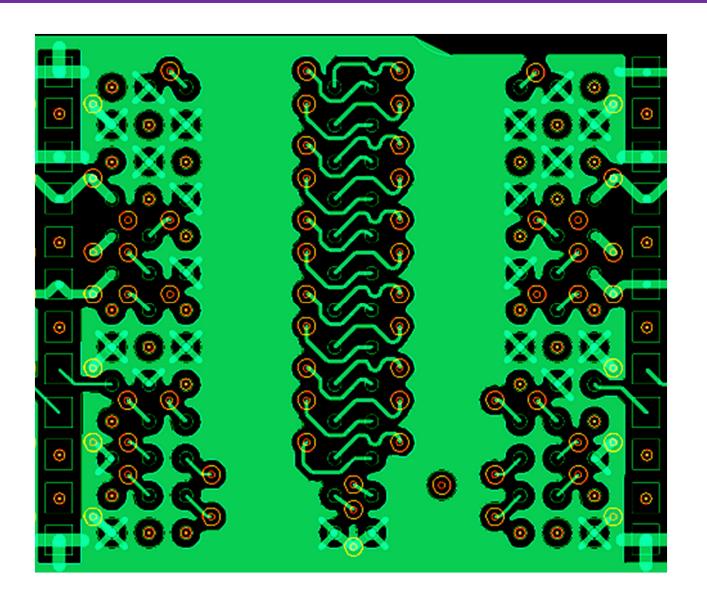DDP

DFD

Are We Out of Tricks?

Layout with Via-in-Pad

Improved power delivery

Reduced inductance

More copper flooding for thermal distribution

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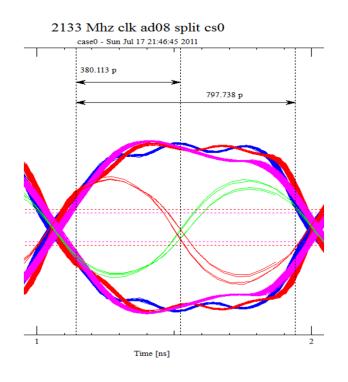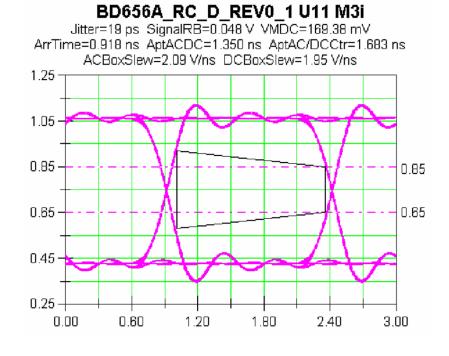# Example Design: 4Rx4 RDIMM

Simple 10 layer design

72 DRAM die

Signal Quality & Frequency

2133 Mhz clk ad08 split cs0
case0 - Sun Jul 17 21:46:45 2011

380.113 p

797.738 p

Time [ns]

BD656A_RC_D_REV0_1 U11 M3i
Jitter=19 ps SignalRB=0.048 V VMDC=169.38 mV
ArrTime=0.918 ns AptACDC=1.350 ns AptAC/DCCtr=1.683 ns
ACBoxSlew=2.09 V/ns DCBoxSlew=1.95 V/ns

Invensas @ 2133
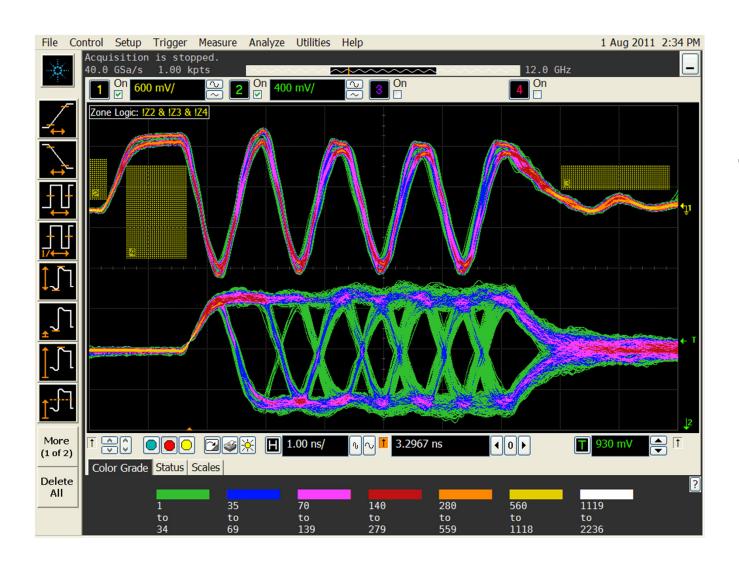
Window = 798 ps

Ideal tCK = 938 ps

85% of a tCK

JEDEC card D @ 1333

Window = 1093 ps

Ideal tCK = 1500 ps

73% of a tCK

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Reality Check

2 DIMMs per channel

Running at DDR3-1600

Conclusions

High speed design limited by "death by a thousand paper cuts"

Using the monolithic ballout for DDPs introduces a lot of paper cuts

Rethinking DRAM stacking leads to new levels of module performance

Signal quality & power delivery can be significantly improved

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Thank You

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