DISCOBOLUS DESIGNS

Embedded Resistor Tolerance – When is it "good enough"?

Embedded resistor technologies provide a large number of obvious advantages over surface mount devices ranging from increased available surface area, reliability improvements, imperviousness to pollutants, improved routing and placement, and on and on. Manufacturing cost savings can even make an embedded resistor solution lower cost than the use of SMT. However, in speaking with potential users in the memory market, the argument that kept coming up was that the tolerance of embedded resistors was "not good enough". This led us to ask the obvious question: what is "good enough"?

Embedded resistor technologies share a common challenge to providing low resistor value tolerances. Due to a number of factors such as copper etchback, PCB weave, and so forth, embedded resistors naturally want to tend to a ±15% tolerance for high yield mass production. Getting to ±5% can be done but typically requires higher cost laser trimming. Since surface mount resistors are generally "free" with a ±5% tolerance, this has led many system designers to avoid embedded resistors for designs that could benefit from them.

Memory subsystems use hundreds of resistors for signal damping and line termination. Common in DDR3 and similar generations of main memory are topologies like the following, with series damping at the outputs of data drivers and parallel termination on the flyby address buses.

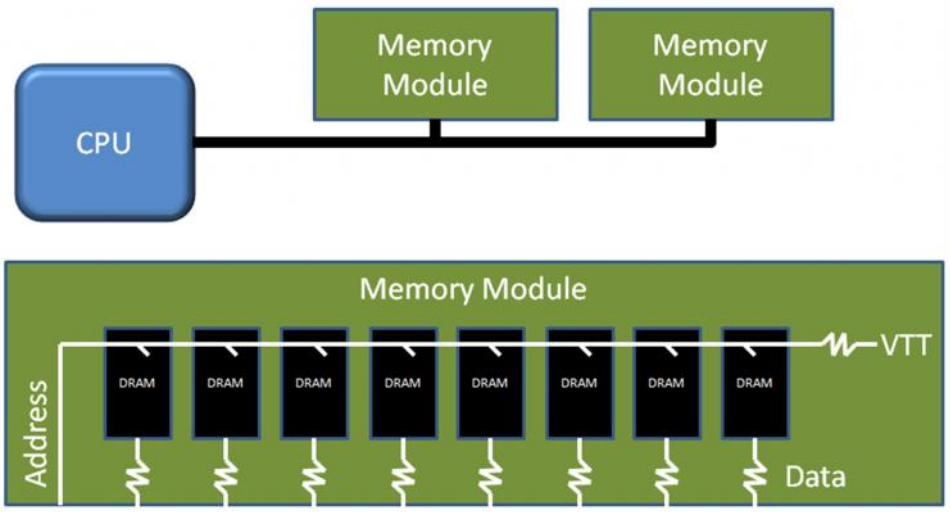

Figure 1: Typical SO-DIMM System Configuration

The concept is to match line impedances and thereby minimize reflections on the bus, increasing signal quality and increasing the operation frequency and reliability. However, these theories are guidelines and in an imperfect world – think of all the sources of errors in attempting to calculate impedance mismatches – the industry finds solutions that solve problems, ship products, and move on to the next challenge. For example, for DDR3, the data series damping resistors are specified as 15Ω and the address termination resistors are specified as 36Ω.

Here's where the line between the solution and the problem got fuzzy. Exactly how much does the value of these resistors affect signal quality? At ±5% tolerance, the range on these resistances is from 14.25Ω to 15.75Ω, and from 34.2Ω to 37.8Ω. Does this mean that the circuits will fail outside that range, say at 13Ω and 40Ω? Answering that question took a bit more homework.

During the design of the world's first standard memory module with embedded resistors, JEDEC DDR3 SO-DIMM raw card J0, Discobolus Designs built a system simulation model including the CPU, motherboard, sockets for two SO-DIMMs per memory channel, and of course the memory module itself. Very aggressive settings were included in the simulation: data rate of 2133 million bits per second, drive strength corner conditions from slow-slow through fast-fast, crosstalk, etc.

In addition, the resistor values in the simulation were tested at extreme settings. For the data resistors we set the values to ±33% (10Ω and 20Ω). Having been warned by others that the address bus amplitude levels might be a concern, we were not quite as aggressive on the address terminations, setting them at ±20% (31.2Ω and 46.8Ω), though in retrospect we had no reason to be so conservative.

The results were conclusive: termination resistor values have negligible impact on signal timing or signal quality.

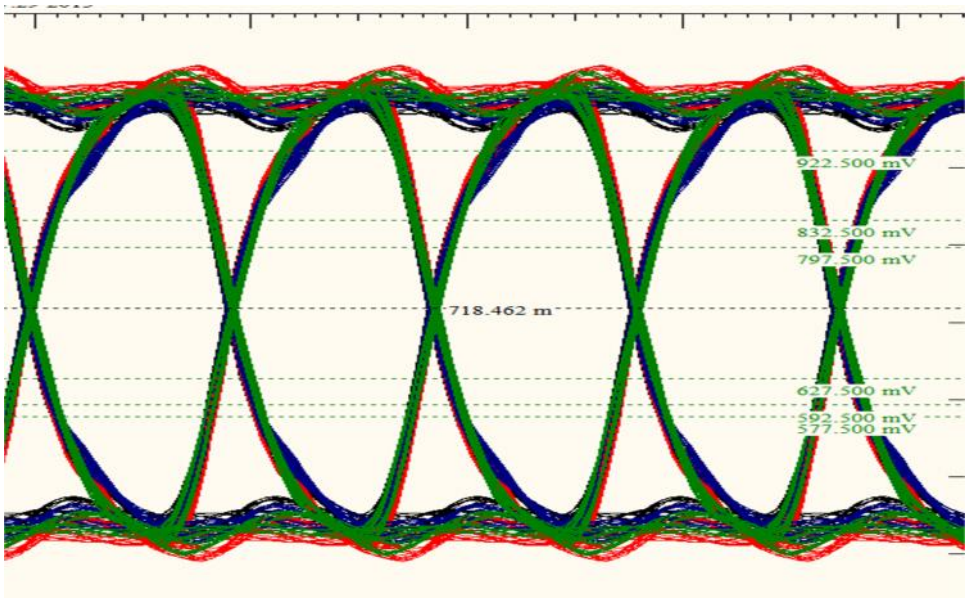

Figure 2: Data Write Cycle @ DDR3-2133

As shown in this simulation of a data write cycle, amplitudes are great, reflections are minimal. Most importantly, the width of the data eye at the interesting voltage levels (VIH and VIL) is quite healthy and passed all requirements for operation at this high frequency. Zooming in on the skew between signals at the extremes (i.e., -33% and +33% of resistor nominal value) we found that the timing difference was 6ps out of a total bit time of 469ps or 1.3% of the total timing budget.

The address bus simulations came out equally as encouraging. Like the data, the eyes were wide open at VIH and VIL, signal amplitudes were well above and below the triggering levels with no significant reflections, and overshoot was not a concern.

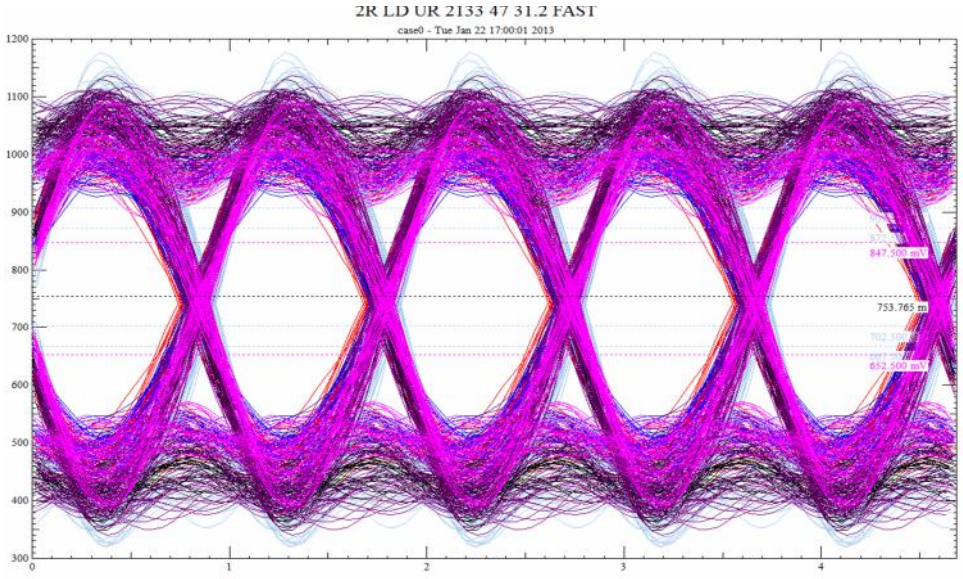

Figure 3: Address Bus Signal @ DDR3-2133

As they say, the proof of the pudding is in the tasting, or in this case, testing. DDR3 SO-DIMM raw card J0 indeed operates well in industry standard computers. The specifications are set to ±15% tolerance for all resistor values, but as stated above, this is to be conservative, leaving additional margin for those intangible system effects.

Figure 4: DDR3 SO-DIMM Raw Card J0

When is resistor tolerance “good enough”? Naturally, each application will make its own determination. For today’s memory applications, untrimmed embedded resistors are definitely “good enough”. In the next article, the question to be raised is “are embedded resistors *better* than SMT?” Spoiler alert: think about signal return paths.

Stay tuned.

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