DISCOBOLUS DESIGNS

Rethinking Signal Integrity Using Embedded Passives

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Agenda

History of memory signal termination

Signal integrity on flyby buses

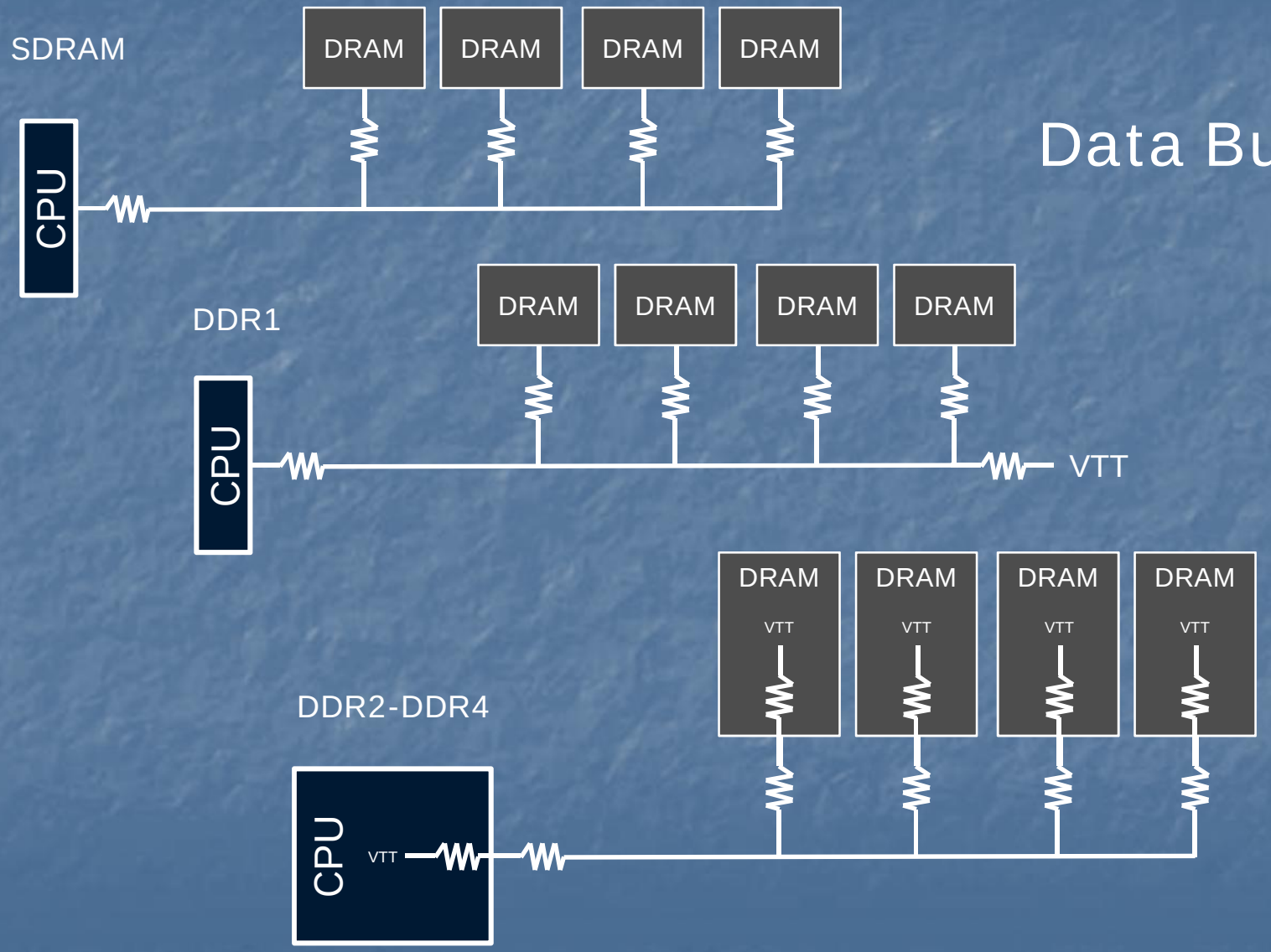
Distributed termination for address buses

Multi-drop socketed buses

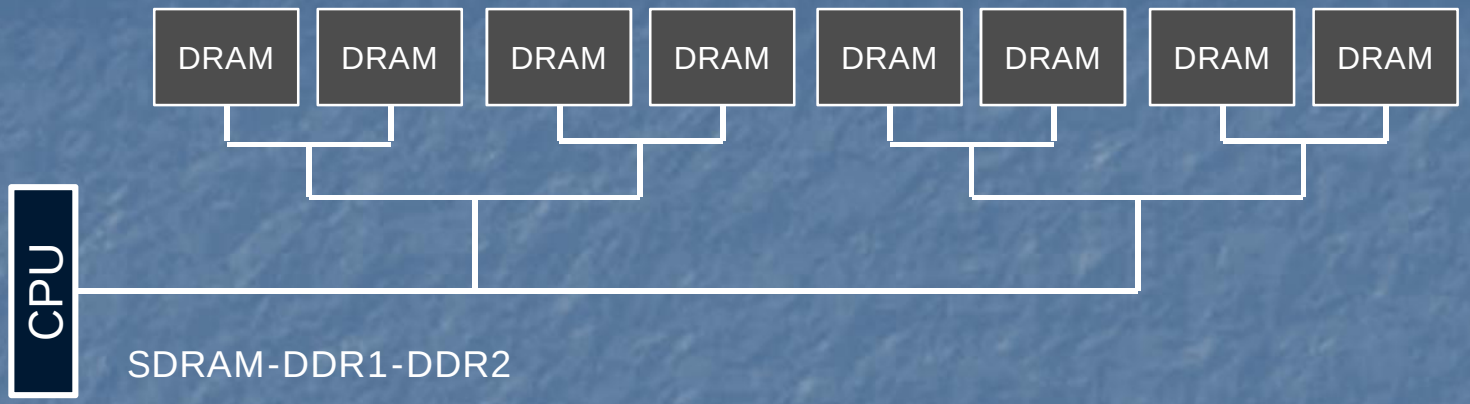
Flyby bus versus branched bus

Line conditioning for multi-drop buses

Memory Bus Signal Termination History

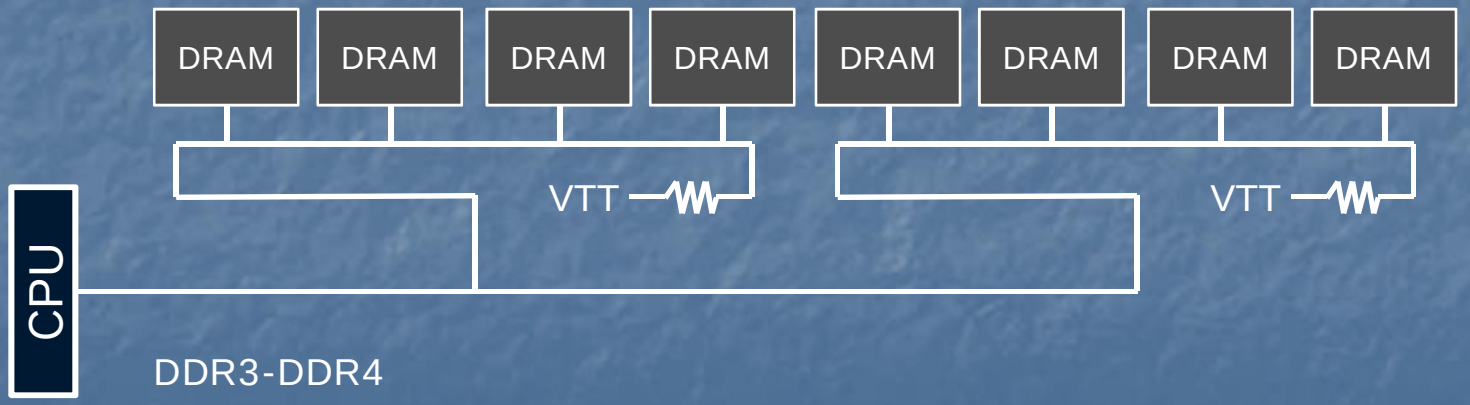


Memory Bus Signal Termination History



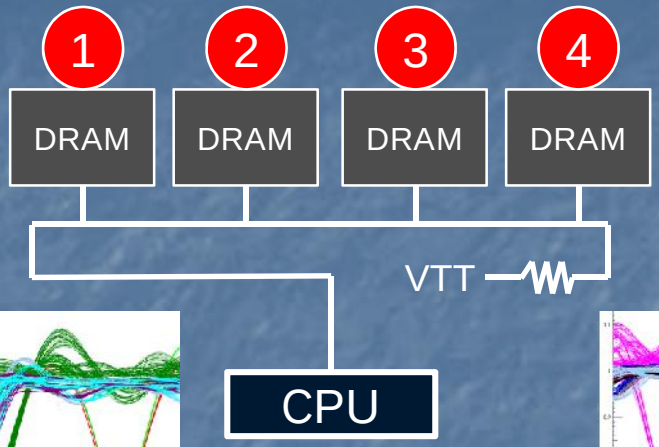
SDRAM-DDR1-DDR2

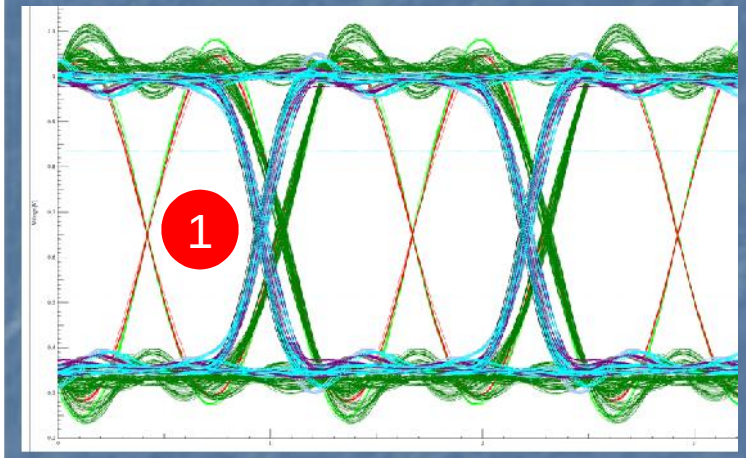
Address Bus

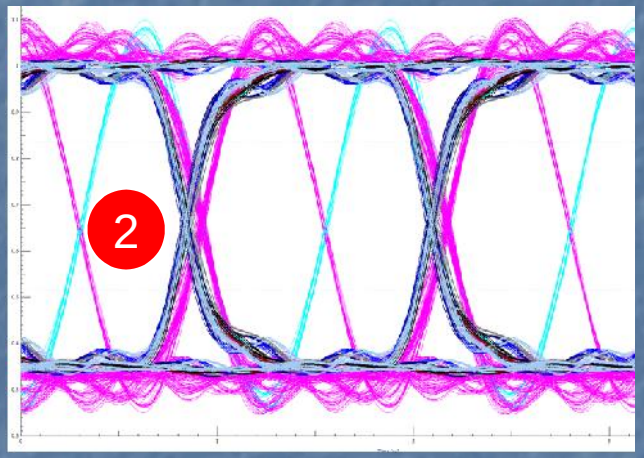


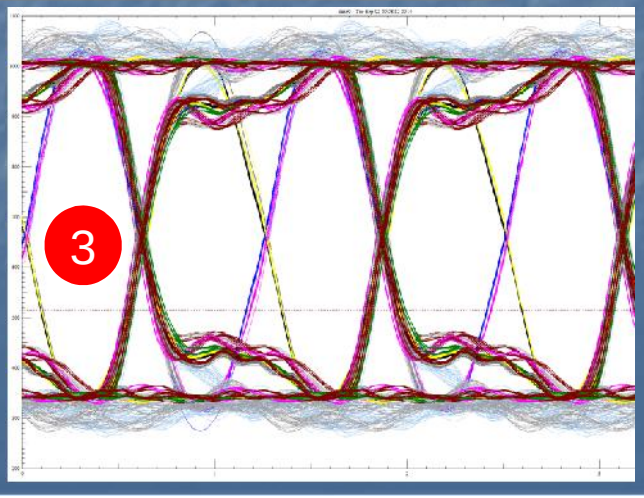
DDR3-DDR4

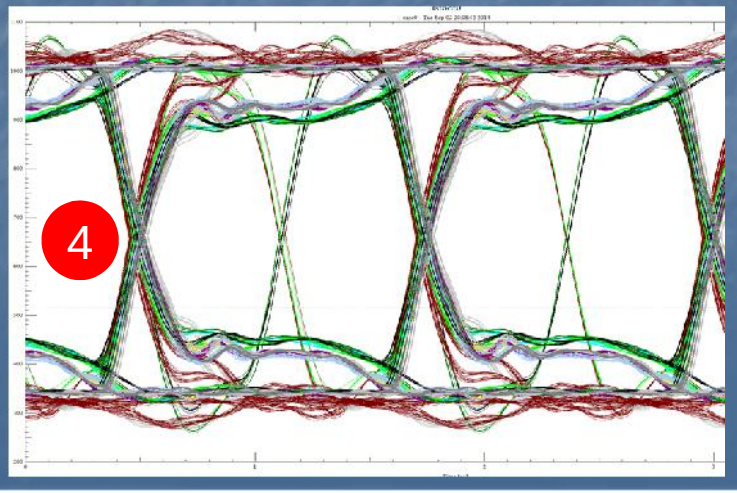
Signal Integrity on the Fly By



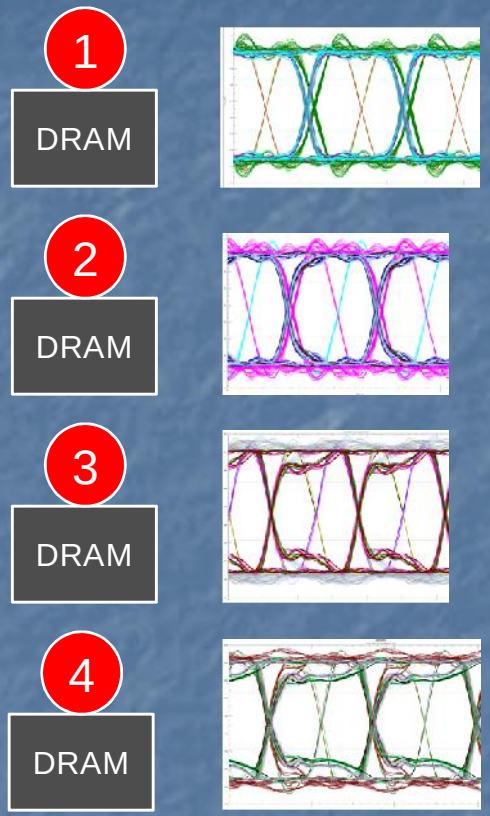








Wishful Thinking



f_{max} = 1136 MHz

f_{max} = 1116 MHz

f_{max} = 1089 MHz

f_{max} = 1066 MHz

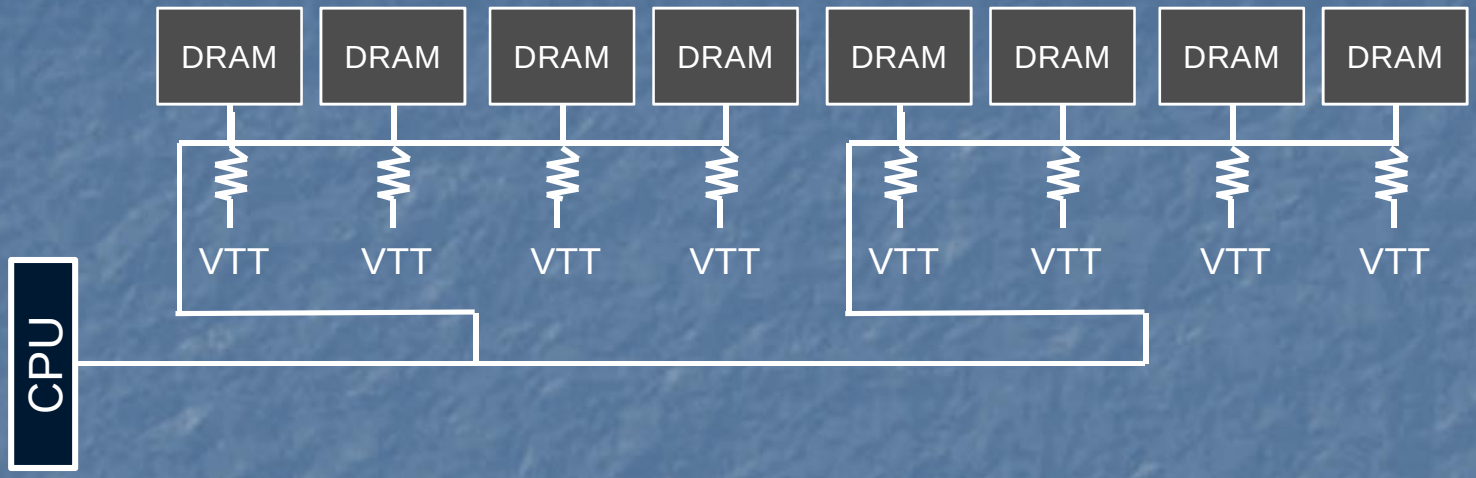
Solution frequency = $(f_1 + f_2 + f_3 + f_4) \div 4$ = 1101 MHz, right?

Of course not…

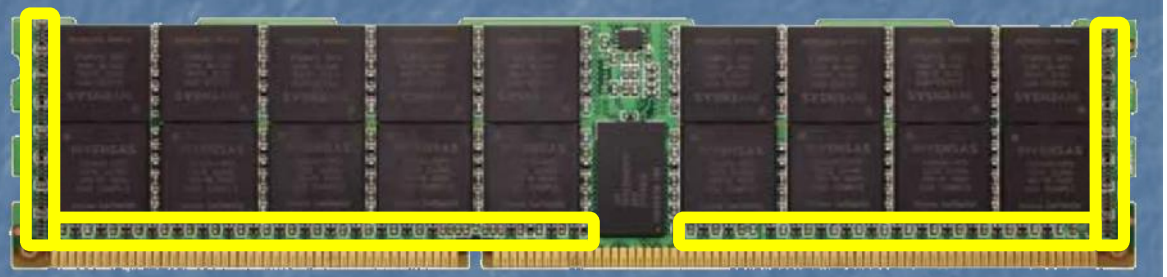
Solution frequency = Min(f_1 .. f_4) = 1066 MHz

So how do we maximize signal integrity at all DRAMs?

Distributed Address Termination

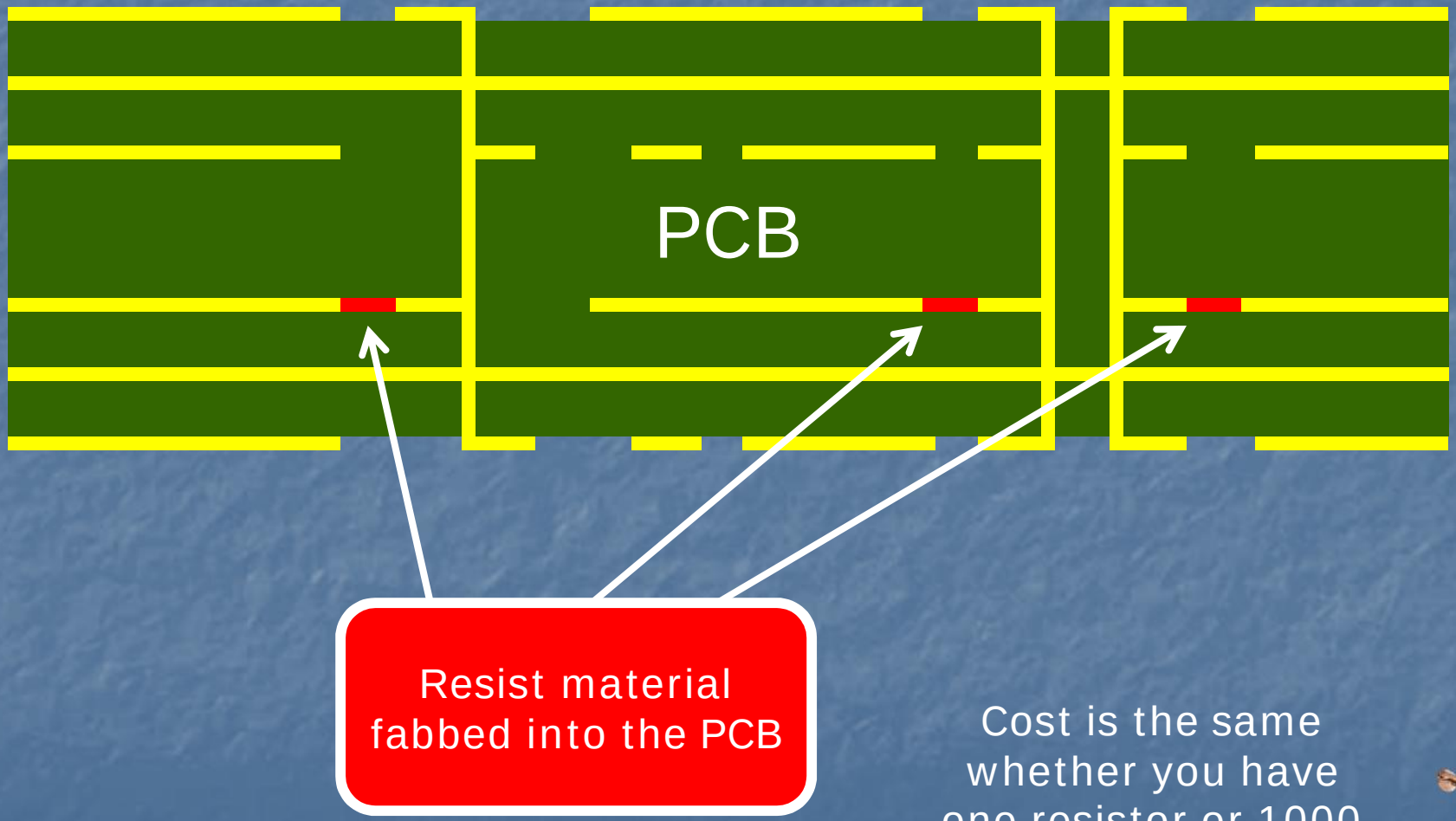


Problem is that termination resistors already take up 20% of available surface area



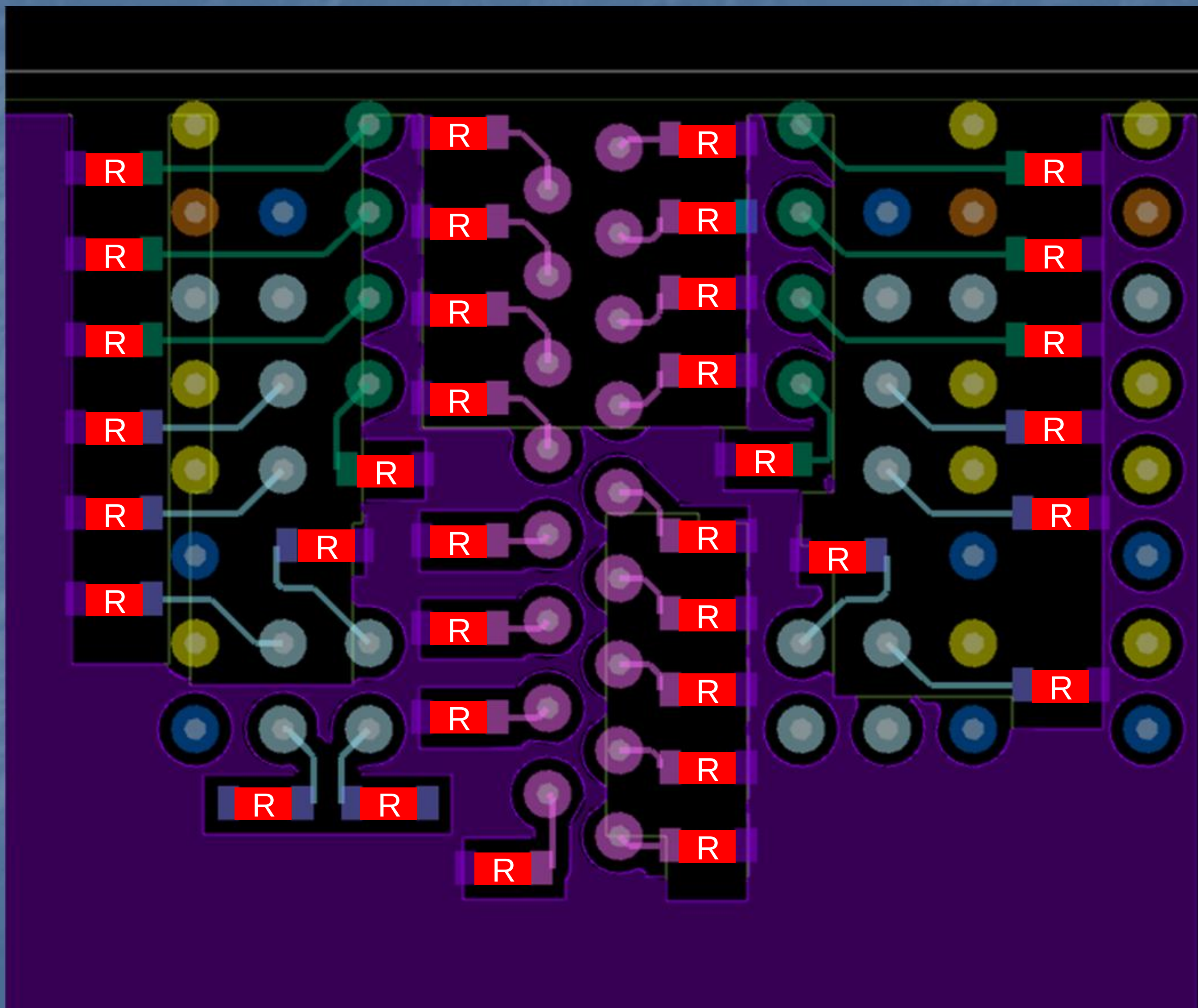
Where would we put these hundreds of resistors?

Embedded Resistor Overview



Cost is the same whether you have one resistor or 1000

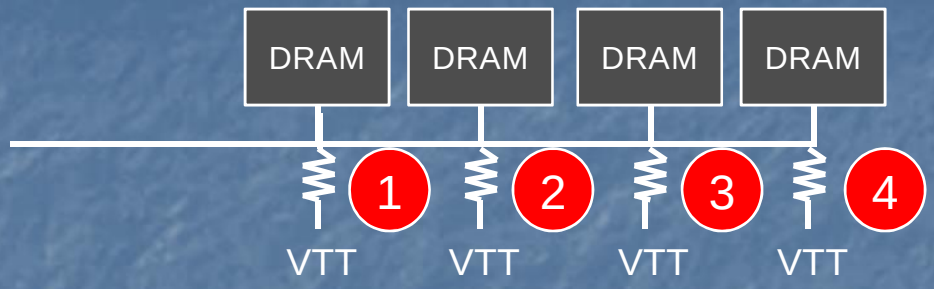
Distributed Termination Using ER



Resistance value is ratio of length to width times base resistance

$$Value = \frac{L}{W} * R$$

Tuning Distributed Termination



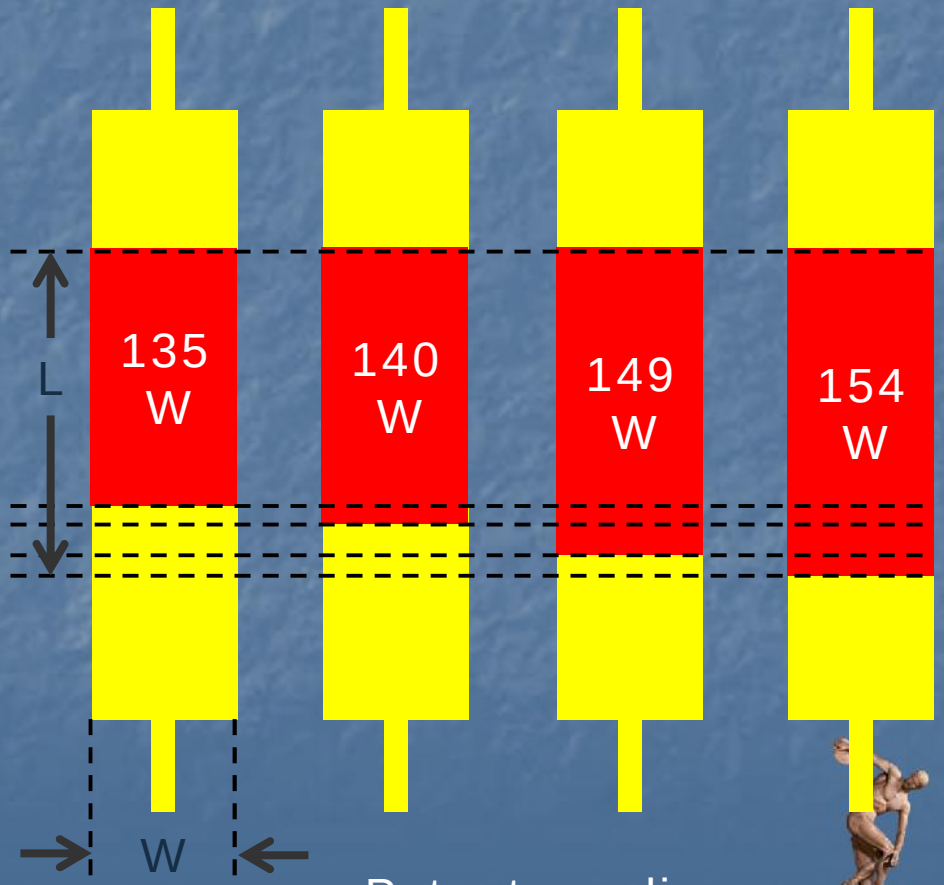
Simple distribution 4 x 36 = 144 W

Tuned distribution (eg only)

R1 = 135 W
R2 = 140 W
R3 = 149 W
R4 = 154 W

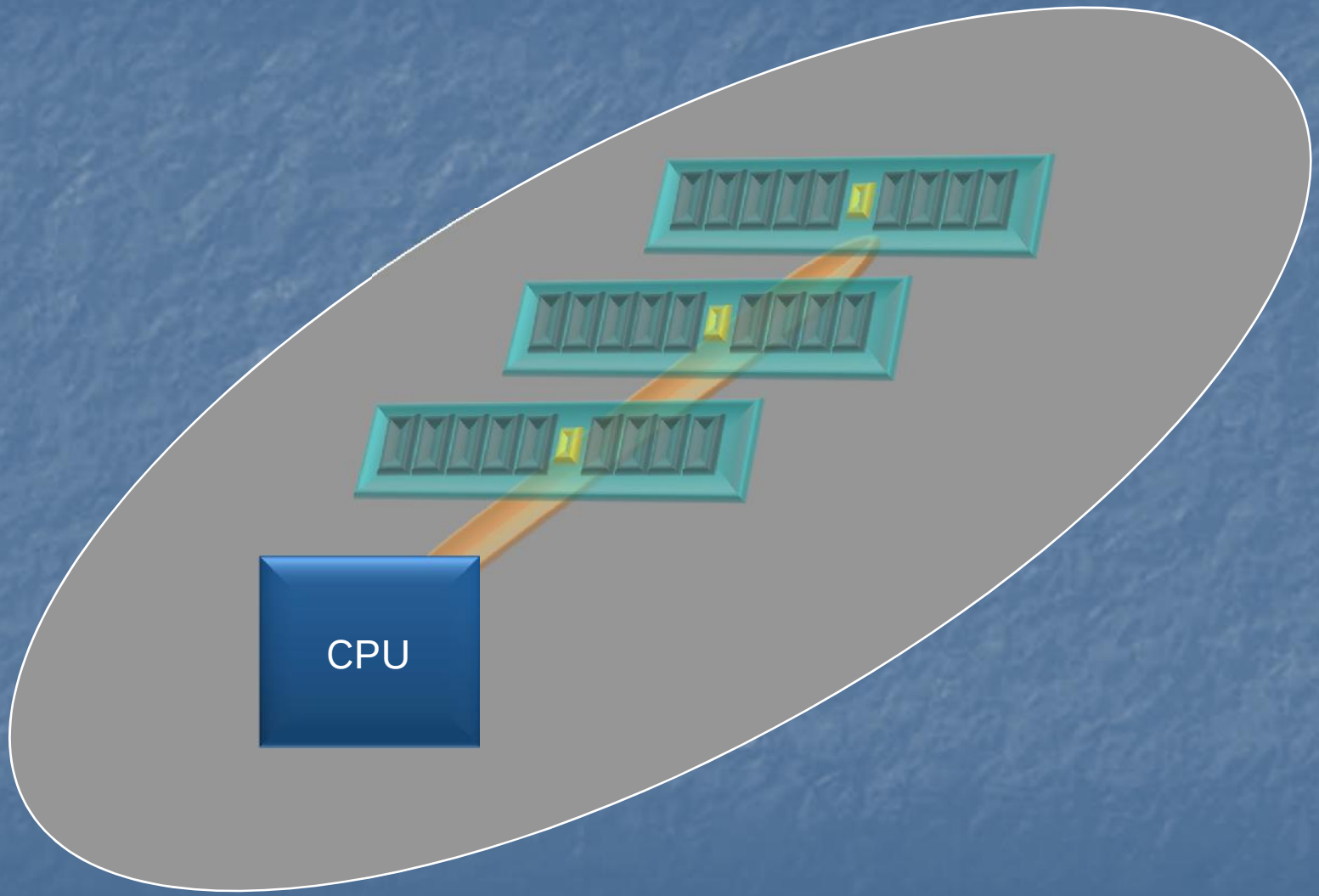
Still 36 Wequivalent, however tuned for signal integrity at each point

Typical termination is 36 W

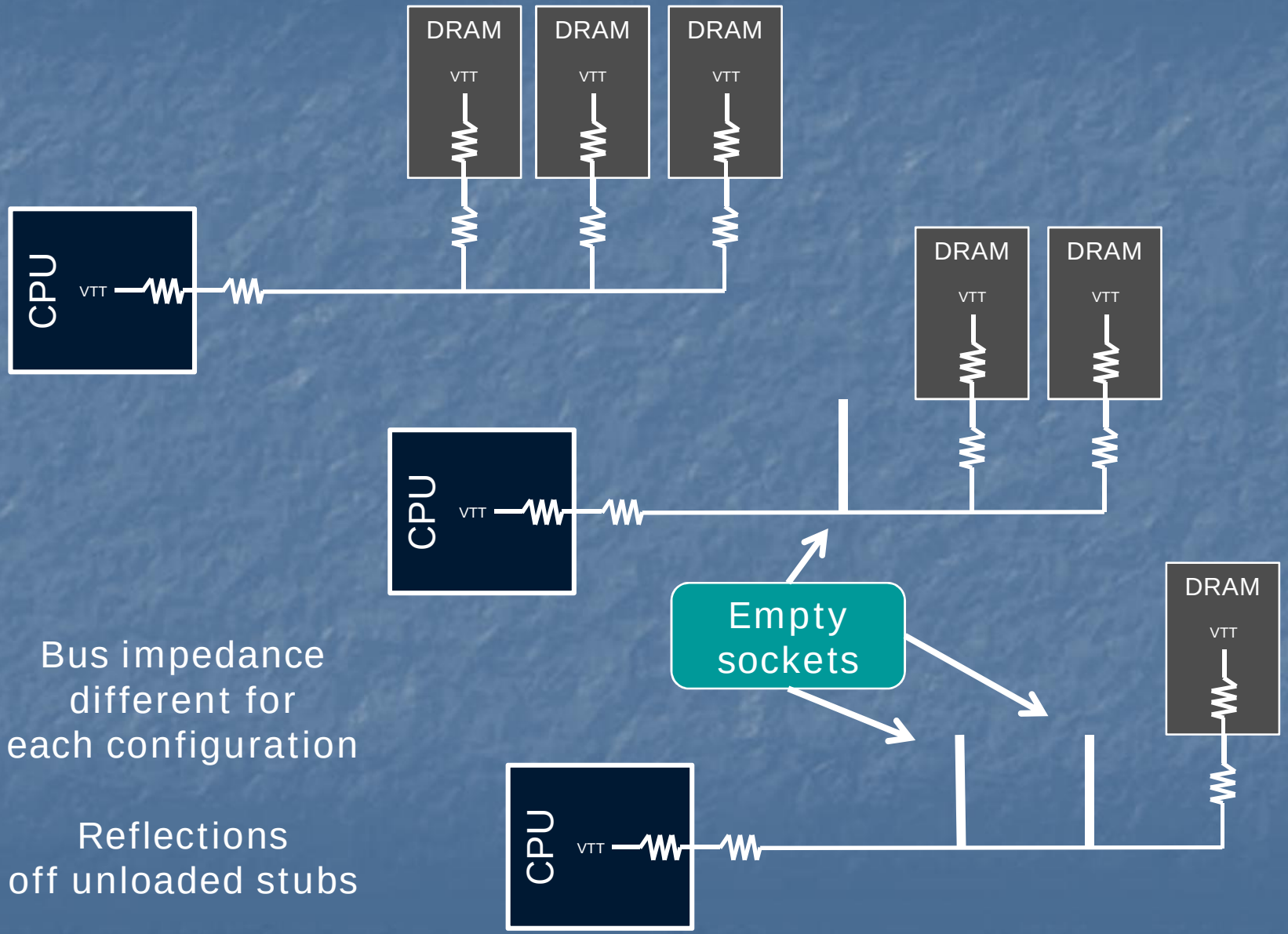


Patent pending

3 DIMMs Per Channel



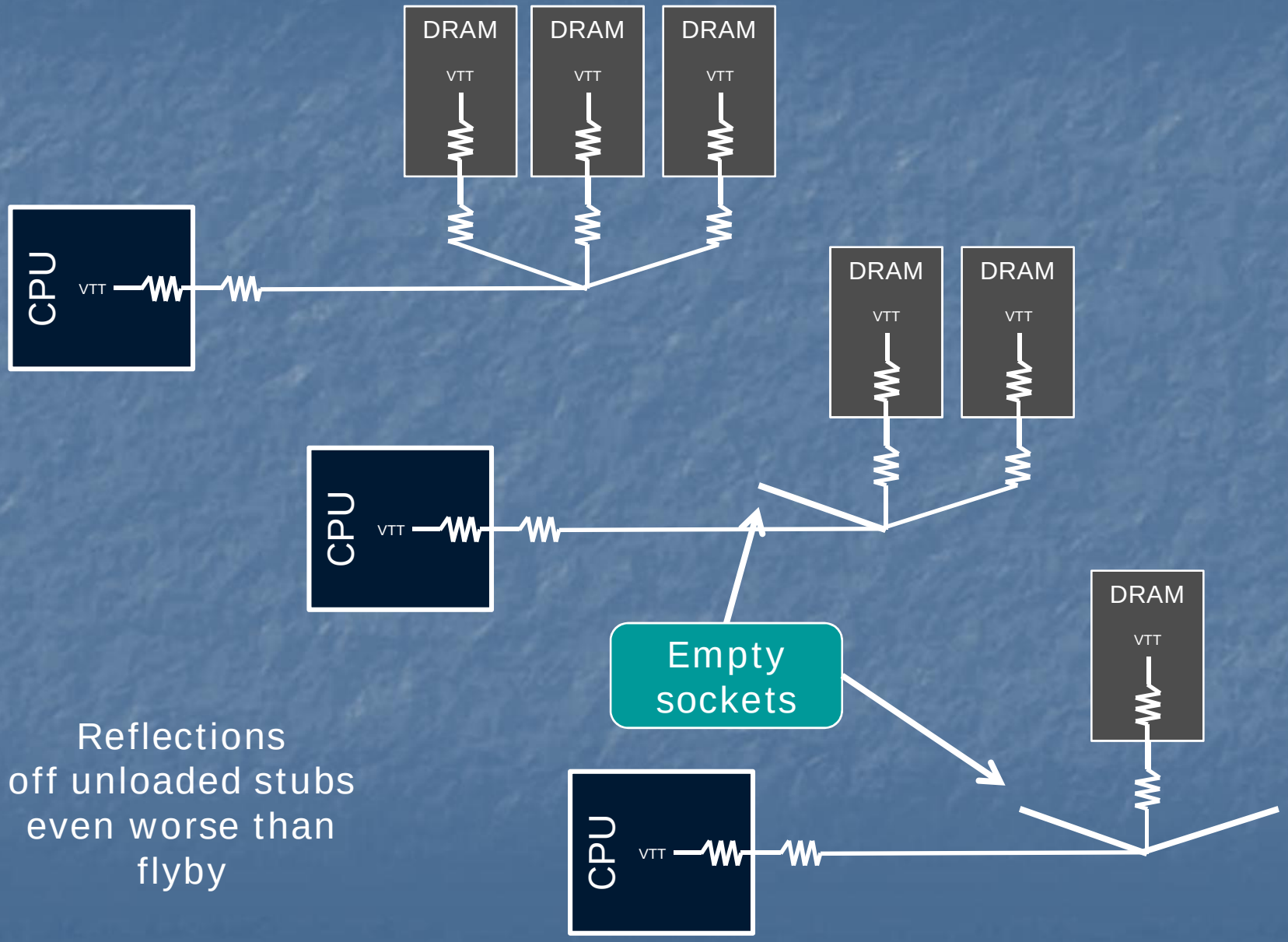
Challenges in Supporting 3DPC



Bus impedance different for each configuration

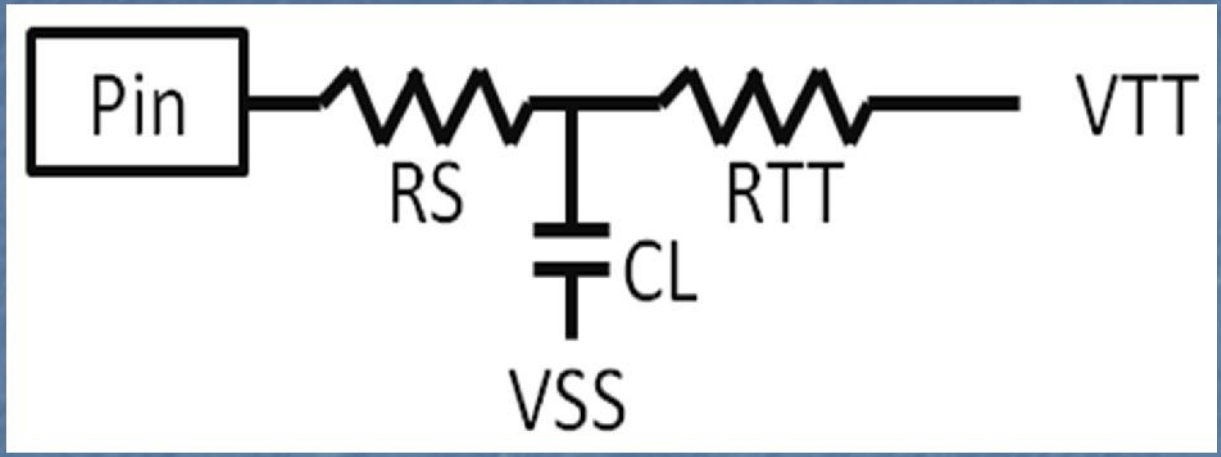
Reflections off unloaded stubs

Desirable Configuration: Branched



Reflections off unloaded stubs even worse than flyby

Line Conditioning Module



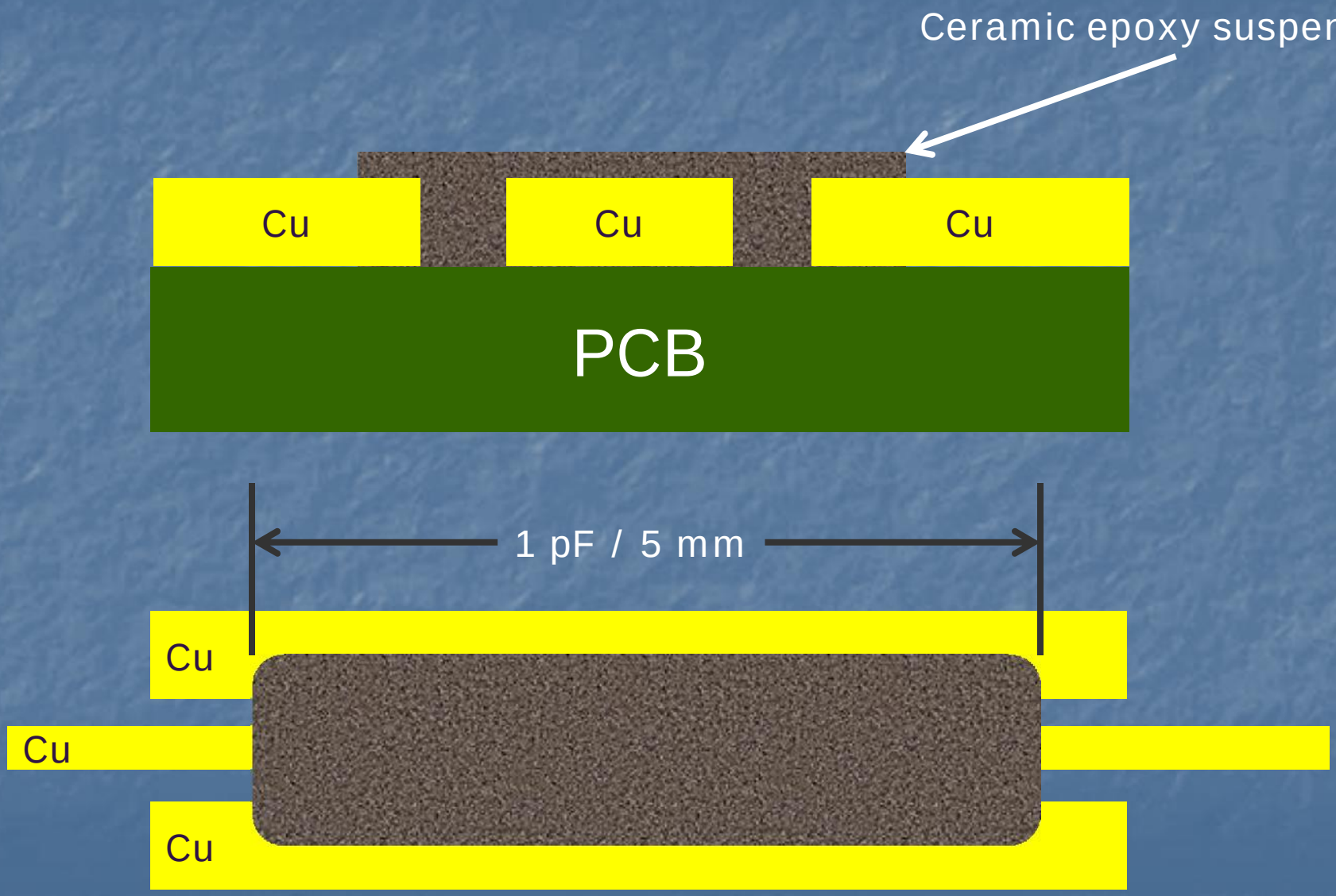
Terminates every active signal on the bus

Values match loading equivalent of 2 rank DIMM

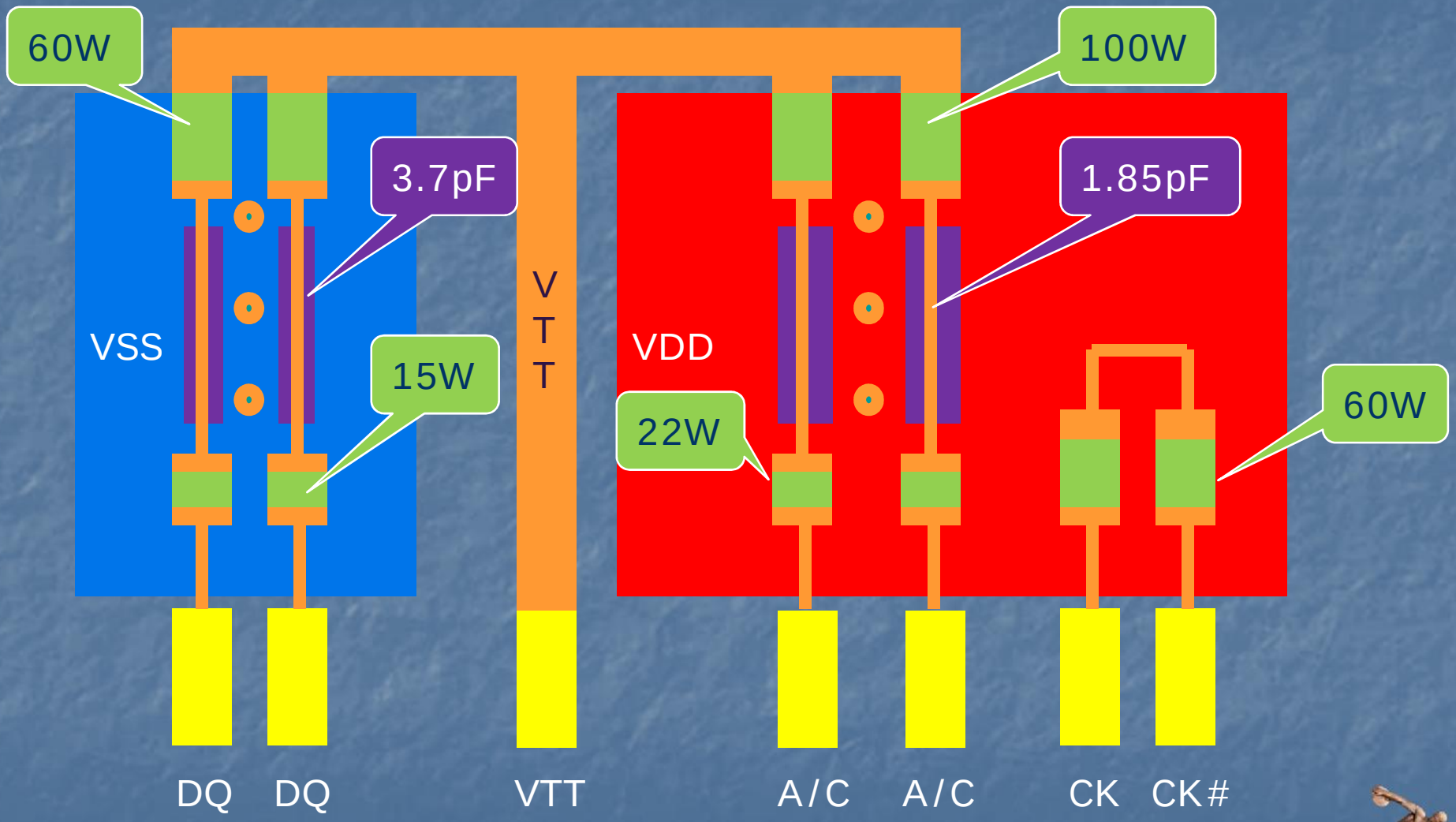
Signal	RS	CL	RTT
Data	15 W	3.7 pF	60 W
Address	22 W	1.85 pF	100 W

DDR3 DIMM example shown

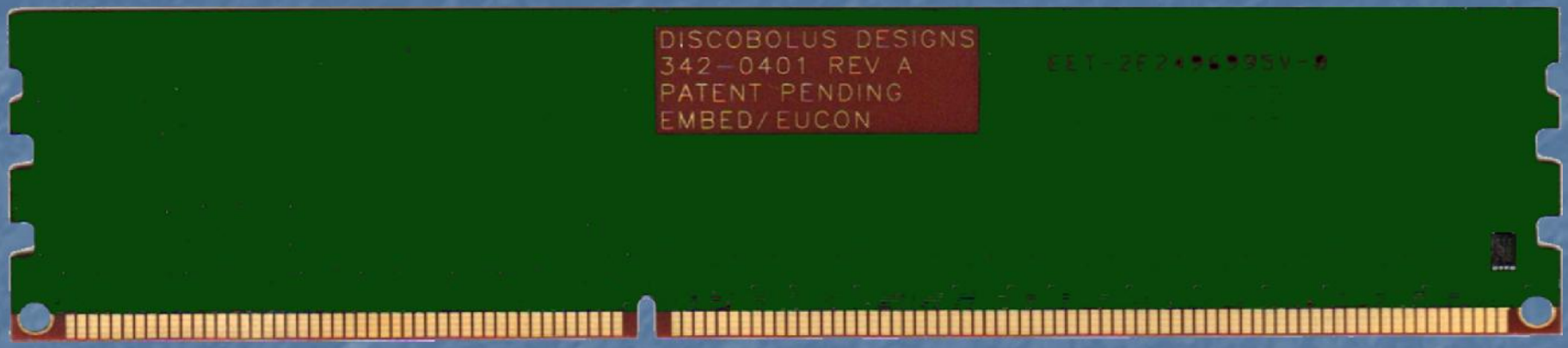
Printed Embedded Capacitor

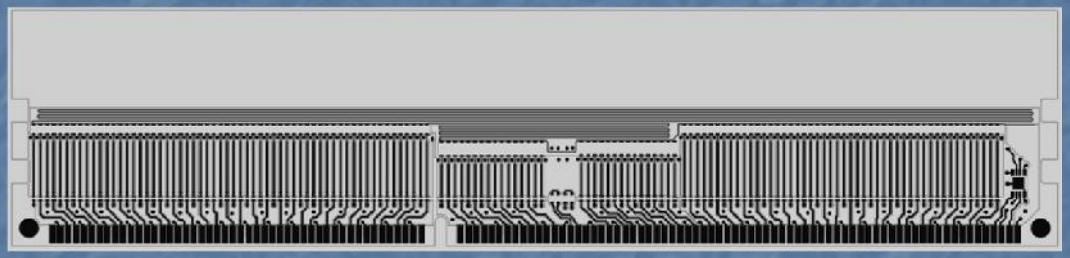


Termination Networks



Line Conditioning Module





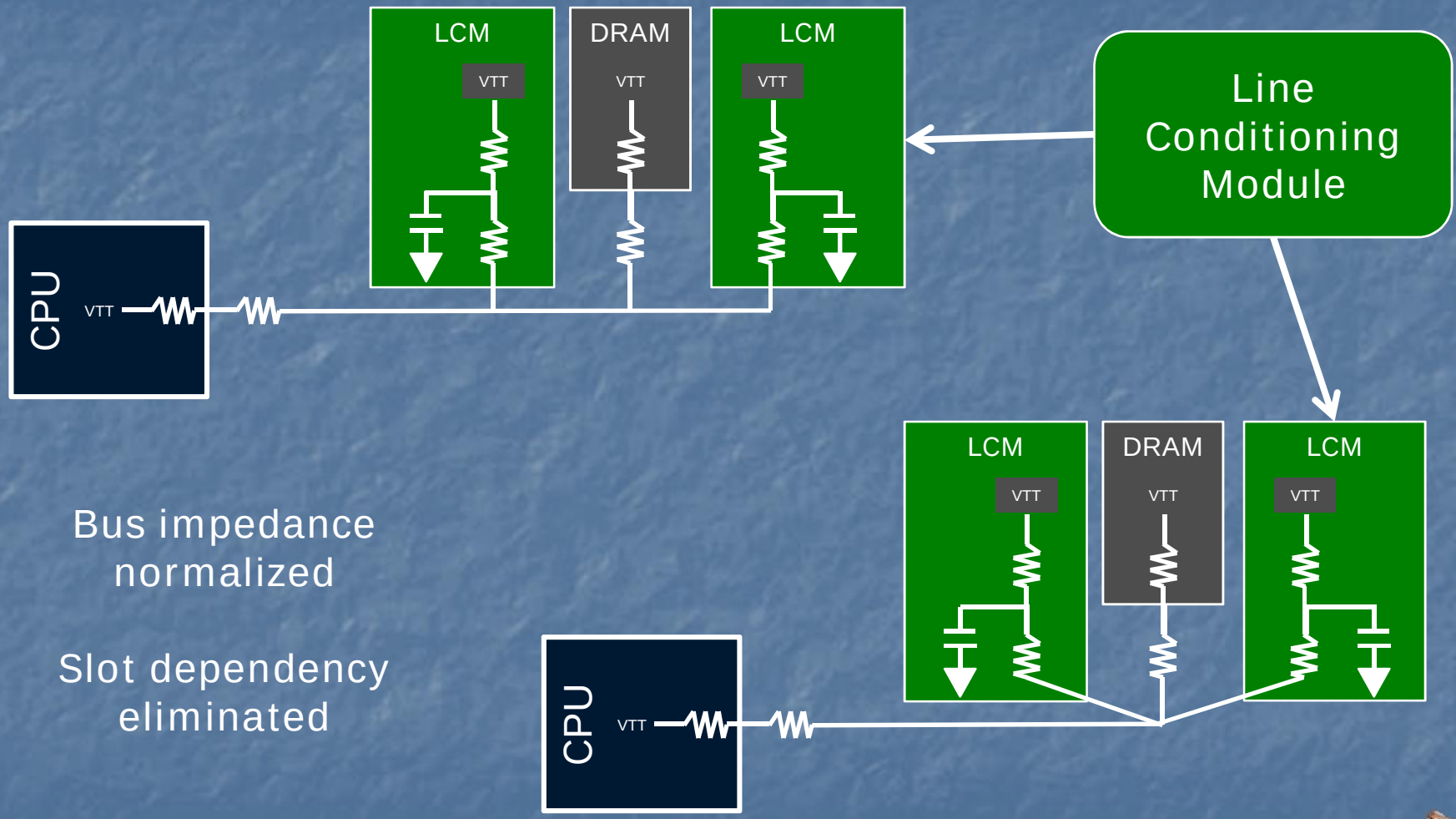
2 layer PCB

300+ Printed resistors

150+ Printed capacitors

Optional SPD: only mounted component
can include thermal sensor

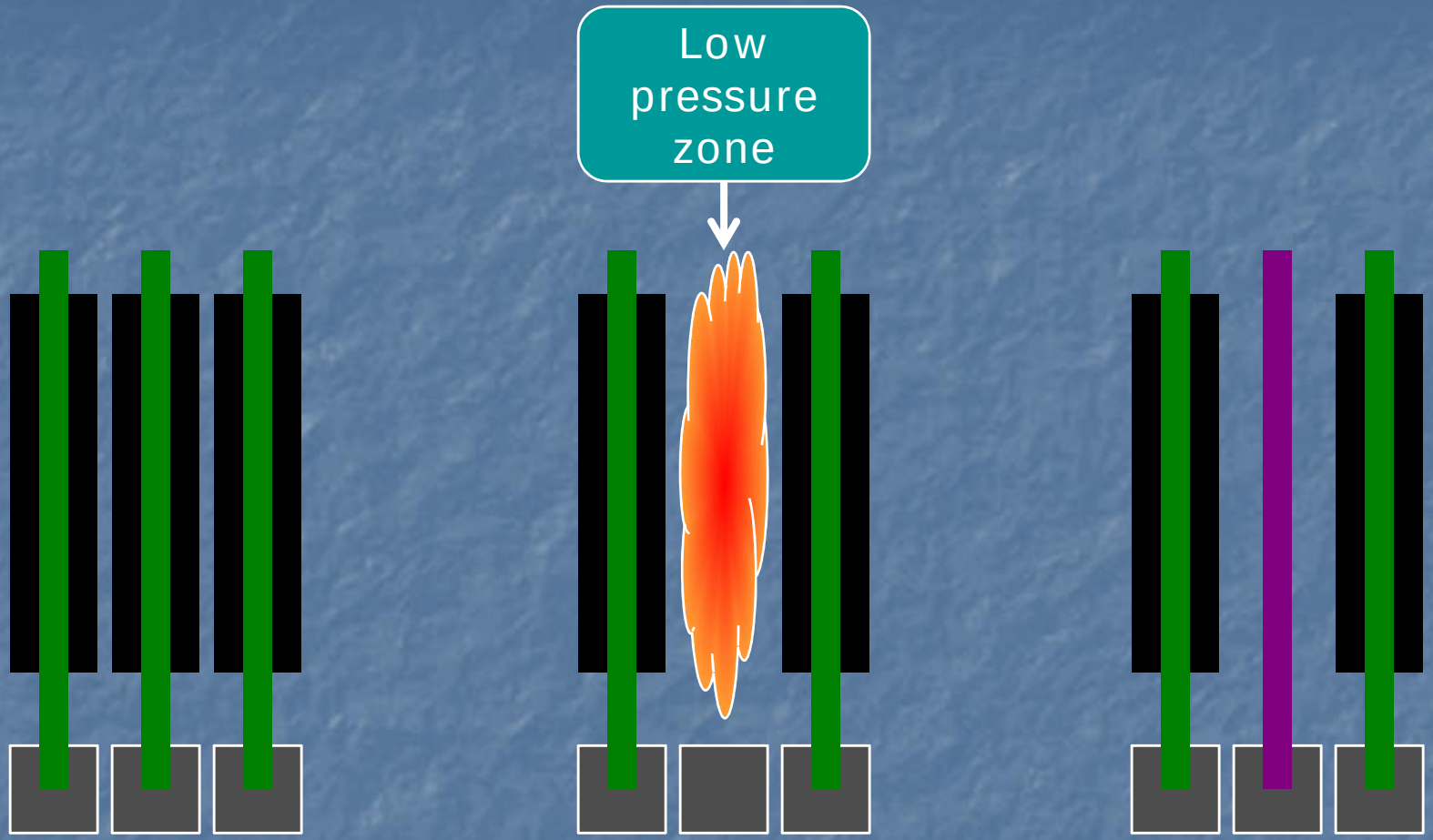
Using Line Conditioning



Bus impedance normalized

Slot dependency eliminated

Nice Thermal Side Effect



Fully populated channel

Empty socket

Line Conditioning module installed

Concluding

Memory bus termination still evolving

Multi-drop socketed buses challenging

Embedded resistors and capacitors provide unique solutions to these problems

Thank you!

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