Embedded Passives in Memory Modules

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Netlist

- Manufacturer of very high density memory modules
- Based on JEDEC industry standards
- Propose new industry standards
  - Chairman of
    - DRAM packaging committee
    - Small Modules committee
    - 4 Rank Module Task Group
- Currently in production with embedded resistors
- Also use embedded capacitors for labs, future production use planned
Performance Requirements

• Today’s DRAM interfaces
  – Running at 400, 533, 667, 800MT/s per pin, 72 bits wide
  – Command rate \( \frac{1}{2} \) of DRAM interface rate

• Next generation (2007)
  – DRAM interfaces to 1600MT/s per pin
  – Controller-hub interfaces at 4.8GHz \( \rightarrow \) 9.6GHz
Why Embedded Passives?

Using embedded resistors

Using SMT resistors

4 mm keepout
Why Embedded Passives?

Saves space for what my customers pay for: DRAMs

Improves signal integrity due to ability to place components where needed

Reduces manufacturing cost – break even at 65 replaced SMT placements

Increases module reliability – eliminates #1 failure mechanism in production
**Very Low Profile Memory Module**

- **Top Gap**: 0.3
- **Res Gap**: 0.3
- **Mem Height**: 12.2

<table>
<thead>
<tr>
<th></th>
<th>Top Gap</th>
<th>Res Gap</th>
<th>Mem Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP</td>
<td>0.3</td>
<td>0</td>
<td>12.2</td>
</tr>
<tr>
<td>0201 res</td>
<td>0.3</td>
<td>1.7</td>
<td>10.5</td>
</tr>
<tr>
<td>0402 res</td>
<td>0.3</td>
<td>2</td>
<td>10.2</td>
</tr>
</tbody>
</table>

**Dimensions**

- **Mem Height**: 13.5
- **DRAM**: 0.35
- **R-pack**: 1.0, 2.7, 3.0
- **Contact**: 1
# DDR2 512Mb BGA Comparison

<table>
<thead>
<tr>
<th></th>
<th>Monolithic</th>
<th>Stack 1</th>
<th>Stack 2</th>
<th>Stack 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>AAA</td>
<td>12x19</td>
<td>12x19</td>
<td>16x20</td>
<td>12x19.2</td>
</tr>
<tr>
<td>BBB</td>
<td>11x13</td>
<td>11x13</td>
<td>15x14</td>
<td>12x13.2</td>
</tr>
<tr>
<td>CCC</td>
<td>11x11.5</td>
<td>11x11.5</td>
<td>15x12.5</td>
<td>12x11.7</td>
</tr>
<tr>
<td>DDD</td>
<td>10x10.5</td>
<td>10x10.5</td>
<td>14x11.5</td>
<td>12x10.7</td>
</tr>
<tr>
<td>EEE</td>
<td>10x11.2</td>
<td>10x11.2</td>
<td>14x12.2</td>
<td>12x11.4</td>
</tr>
<tr>
<td>FFF</td>
<td>12x14</td>
<td>12x14</td>
<td>16x15</td>
<td>12x14.2</td>
</tr>
<tr>
<td>GGG</td>
<td>11.3x13.8</td>
<td>11.3x13.8</td>
<td>15.3x14.8</td>
<td>12x14.0</td>
</tr>
</tbody>
</table>

All DRAM sizes are different
## DDR2 VLP FrameDIMM

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<tr>
<td>EP</td>
<td>0201</td>
<td>0201</td>
<td>0201</td>
<td>0201</td>
</tr>
<tr>
<td>CCC</td>
<td>DDD</td>
<td>CCC</td>
<td></td>
<td>CCC</td>
</tr>
<tr>
<td>DDD</td>
<td>EEE</td>
<td>DDD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EEE</td>
<td></td>
<td>EEE</td>
<td></td>
<td>EEE</td>
</tr>
</tbody>
</table>
Embedded Capacitor Geometries

Future needs
-----
3 nF/mm² evaluation in 1Q05

- Need small micron to sub-micron dielectrics

- Using rolled on CFP (Motorola process)
Probing BGA-based designs
DRAM Load Simulator (DLS)

- BGA substrate with DRAM footprint below
- Top surface has probe points for all signals
- Per-signal internal load matching pF-class capacitors
Load Matching 1:2 Register Outputs

• With 18 DRAM sites, hard to balance as 9+9 loads
  ∴ Tight layouts often have 10+8 loads

• Embedded 2X strength DLS can balance both sides
Reliability of Embedded Resistors

- Screened polymer thick film, Motorola process
- One value of ink (50$\Omega$), one screening
- 110 resistors @ 22$\Omega$ nominal
- 20 resistors @ 60$\Omega$ nominal
## Summary of Life Tests

<table>
<thead>
<tr>
<th>Bare Boards</th>
<th>Assembled Boards</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Exhibit A: Testing the same resistors through 2 refows, a bake, then 10 more refows</td>
<td>• Exhibit E: Biased humidity testing</td>
<td>• Exhibit F: Impact on system timing at margin</td>
</tr>
<tr>
<td>• Exhibit B: Heat soak, thermal cycle, humidity</td>
<td></td>
<td>• Exhibit G: Tolerance push to failure</td>
</tr>
<tr>
<td>• Exhibit C: Testing the same resistors over repeated thermal cycling</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Exhibit D: 3-axis vibration</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Buried Resistor Tolerance Over Thermal Shock

Purpose: Six resistors per board tested at multiple cycle points during heat testing, all 110 resistors tested before and after thermal stress

1. Measure resistance
2. Reflow @ 220 °C
3. Measure
4. Reflow @ 220 °C
5. Measure
6. 55 °C bake for 12 hours
7. Measure
8. Reflow 10 times @ 220 °C
9. Measure
All Boards, All Resistors

Average:

$\Delta = -0.1 \, \Omega, \, 2 \text{ refloows}$

$\Delta = -0.5 \, \Omega, \, 12 \text{ refloows}$
Buried Resistor Tolerance Under Thermal Stress

Purpose: Application of heat soak, thermal cycle, and humidity

Heat soak: 150°C
Thermal cycle: -10°C to +115°C @ 3°C/minute
Humidity: RH 85% at 85°C, module powered to 2.5V
Embedded Resistors: Thermal Shock

Conditions:
500 hours of heat soaking

Conditions:
500 hours of thermal cycling

Conditions:
500 hours of humidity stress
Buried Resistor Tolerance and Drift & Analyze Probing Accuracy

Purpose: Analyze drift for same resistors over 500 thermal cycles on the same board. Analyze tester tolerance.

Method: Thermal cycle: -10°C to +115°C @ 3°C/minute
Resistor Values Over Cycling

- +15% (25.3Ω)
- +10% (24.2Ω)
- Nom (22Ω)
- -10% (19.8Ω)
- -15% (18.7Ω)

No average drift over hundreds of thermal cycles
Resistor Sampling Error

<table>
<thead>
<tr>
<th></th>
<th>0 Hrs</th>
<th>168 Hrs</th>
<th>Retest</th>
<th>Retest</th>
</tr>
</thead>
<tbody>
<tr>
<td>21.8</td>
<td>21.0</td>
<td>21.2</td>
<td>20.8</td>
<td>21.1</td>
</tr>
<tr>
<td>21.6</td>
<td>21.5</td>
<td>21.1</td>
<td>20.9</td>
<td>21.5</td>
</tr>
<tr>
<td>21.6</td>
<td>20.7</td>
<td>20.8</td>
<td>20.9</td>
<td>21.3</td>
</tr>
<tr>
<td>21.5</td>
<td>20.9</td>
<td>20.7</td>
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<td>21.2</td>
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</tbody>
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Average:

- +15% (25.3Ω)
- +10% (24.2Ω)
- Nom (22Ω)
- -10% (19.8Ω)
- -15% (18.7Ω)
Buried Resistor Vibration Screening

Purpose: Determine impact of mechanical stress on buried resistors due to vibration shock in 3 axes

Method: Tri-axial random vibration system from 0 to $20G_{\text{RMS}}$ in 5G increments, 30 minutes at each stage
Vibration Testing

• 30 modules selected from 5 panels
• 118 resistors checked per module
• 3540 resistance measurements taken for errors caused by vibration at each stage
• 17700 total checks

• Zero Failures Detected
Buried Resistor Biased Humidity Test of Assembled Modules

Purpose: Verify module functionality after temperature and humidity stress with applied voltage bias; look for migration of resist material

Method: 85°C/85% RH
500 Hours
Design Rules for Buried Resistors

PTF BURIED RESISTORS (Motorola Process)

- 3 MIN TRACE
- SILVER LAND AREA
- PTF RESISTOR MATERIAL
- 10 MIN (from resistor to any copper)
- 10 MIN
- 15 MIN
- 20
- 32
- 24
- (3 mil from antepad to trace)
- ANTIPAD FEEDTHRU

<table>
<thead>
<tr>
<th>Width (W)</th>
<th>Length (L)</th>
<th>OHMS</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MILS</td>
<td>11</td>
<td>25</td>
<td>22</td>
</tr>
</tbody>
</table>

Note: All dimensions are in mils
Summary for Exhibit E Testing

- No failures detected
- No visual evidence of erosion
- No visual evidence of filament growth

- Conclusion: No evidence of problems with voltage biased humidity testing
Buried Resistor Tolerance
Timing Impact, Simulation

Purpose: Analyze impact of 20% resistor tolerance

Method: Compare 22 Ω ±20% to JEDEC standard 22 Ω ±5%

Series damping on data and strobe
Timing Comparison

JEDEC:

**WRITES:**
$tDV = 2.24$ ns

**READS:**
$tDV = 2.71$ ns

Netlist:

**WRITES:**
$tDV = 2.24$ ns

**READS:**
$tDV = 2.71$ ns

Conclusion: Identical timing within <10ps in critical voltage region
Buried Resistor Tolerance Pushed to Failure, Simulation

Purpose: Determine how far embedded resistor tolerance can drift before system failure occurs

Method: Simulation of DDR2 system environment to slow/slow and fast/fast corners with resistor tolerance beyond design guardband spec of ±20%
### Summary for Push to Failure Simulation

- **Writes:**

<table>
<thead>
<tr>
<th>Δt normalized (ps)</th>
<th>-50%</th>
<th>-30%</th>
<th>-10%</th>
<th>Nom</th>
<th>+10%</th>
<th>+30%</th>
<th>+50%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Up</td>
<td>↓</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>+60</td>
<td>+50</td>
<td>+40</td>
<td>+50</td>
<td>-10</td>
<td>+10</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **Reads:**

<table>
<thead>
<tr>
<th>Δt normalized (ps)</th>
<th>-5</th>
<th>-4</th>
<th>-1</th>
<th>-2</th>
<th>0</th>
<th>-2</th>
<th>0</th>
<th>0</th>
<th>+2</th>
<th>0</th>
<th>+6</th>
<th>+4</th>
<th>+13</th>
<th>+7</th>
</tr>
</thead>
</table>
Summary

• Exhibit A: Reflow (Bare board)
  – 0.5% drift with normal stress, 2.3% extreme stress
• Exhibit B: Soak, cycle, humidity (Bare board)
  – Tolerance acceptable over stresses
• Exhibit C: Value drift (Bare board)
  – No detectable drift over stress, probing accuracy 0.5 Ω
• Exhibit D: Vibration (Bare board)
  – No failures detected
• Exhibit E: Biased humidity (Assembled board)
  – No failures detected
• Exhibit F: System timing (Simulation)
  – Meets JEDEC standard timing
• Exhibit G: Push to failure (Simulation)
  – System timing should be okay at ±30% or better
Current Status

• Production for over a year
• Many tens of thousands of boards shipped

• Zero failures in manufacturing*

• Zero failures in customer base*

* Attributable to embedded passives
Next Steps

• Better simulation models for buried components

• Improve resistor tolerance <10% without trimming

• Replace decoupling caps (90-ish @ 100nF)
  – Two per DRAM: VDD & VREF
  – 10x10mm footprint
  – Using one layer of capacitors for both sides of the board