# DRAM Module Market Overview


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SimpleTech



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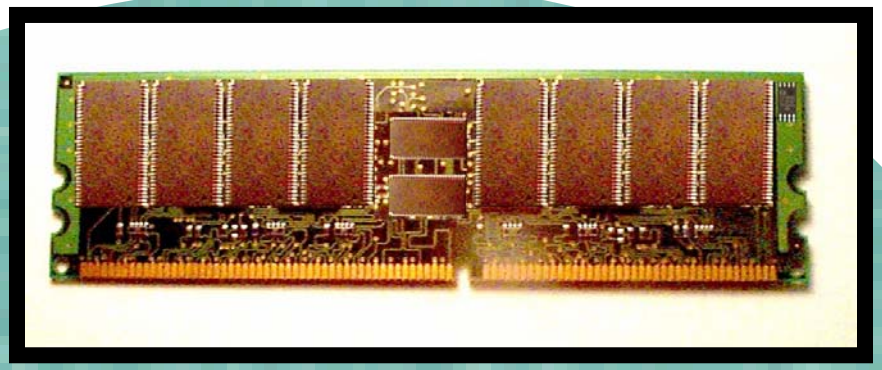
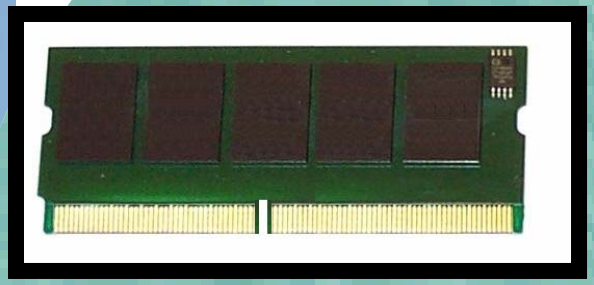
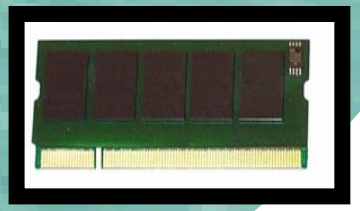
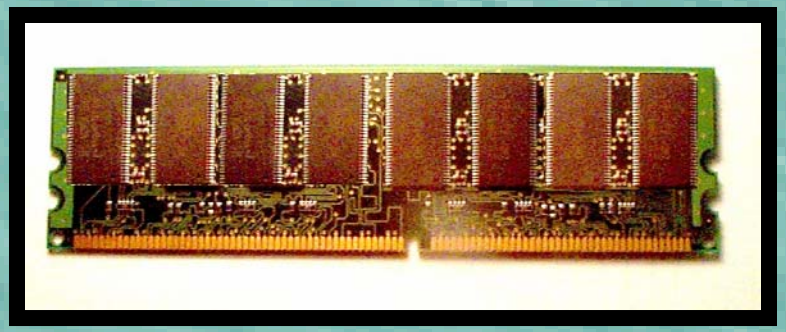
# Many Applications,

# Many Configurations









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# Agenda

- Terminology review
- DRAM Market Factors
- Market:  Personal Computers
- Market:  Servers & Workstations
  - FB-DIMM or RDIMM?
- Market:  Routers & Communications
- Market:  Peripherals



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# DDR2 Speed Grading

| Clock Speed | Chip Bin | Data Rate | Module Bin |
|---|---|---|---|
| 200 MHz | DDR2-400 | 400 MT/s | PC2-3200 |
| 266 MHz | DDR2-533 | 533 MT/s | PC2-4200 |
| 333 MHz | DDR2-667 | 667 MT/s | PC2-5300 |
| 400 MHz | DDR2-800 | 800 MT/s | PC2-6400 |

X64/x72 bit data bus * chip speed



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# DDR3 Speed Grading

| Clock Speed | Chip Bin | Data Rate | Module Bin |
|---|---|---|---|
| 400 MHz | DDR3-800 | 800 MT/s | PC3-6400 |
| 533 MHz | DDR3-1066 | 1066 MT/s | PC3-8500 |
| 667 MHz | DDR3-1333 | 1333 MT/s | PC3-10600 |
| 800 MHz | DDR3-1600 | 1600 MT/s | PC3-12800 |

X64/x72 bit data bus * chip speed



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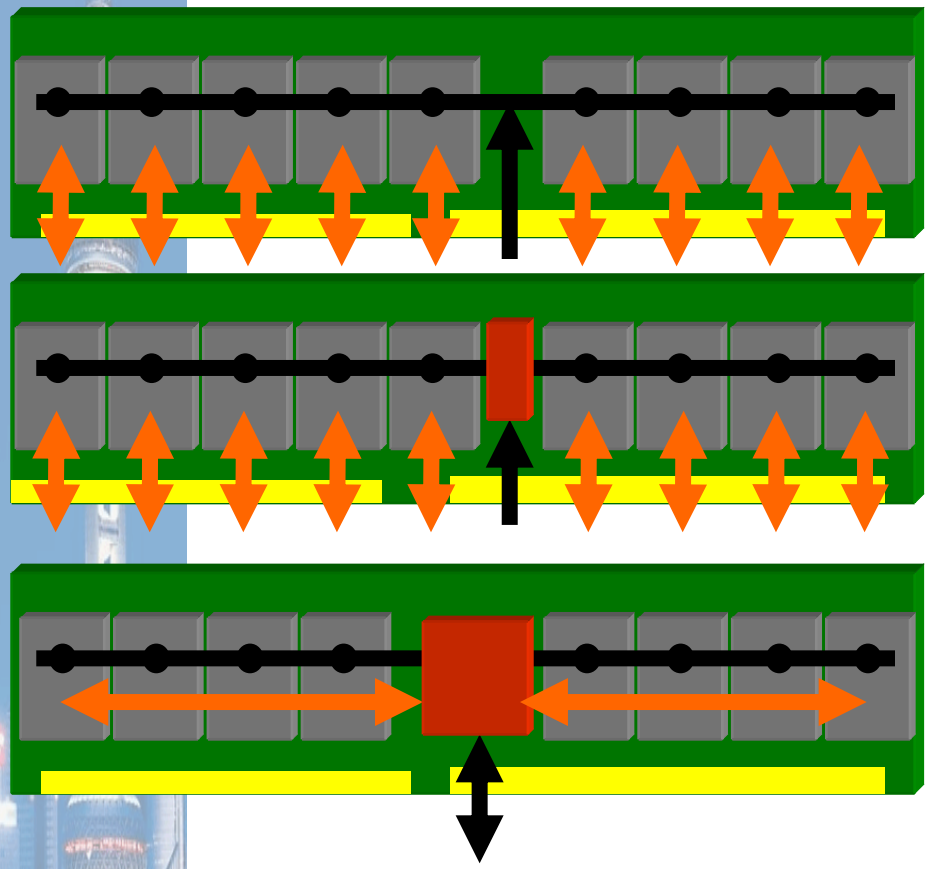
# Terminology

## DIMM = Dual Inline Memory Module



- UDIMM = Unbuffered: Address bus connected directly to DRAMs, limited to 18 chips per DIMM, 2 slots
- RDIMM = Registered: Address bus redriven to DRAMs, enables 72 DRAMs per DIMM, 2 slots
- FB-DIMM = Fully Buffered: Address and data buses packetized and redriven to DRAMs, enables 36 DRAMs per DIMM, 8 slots



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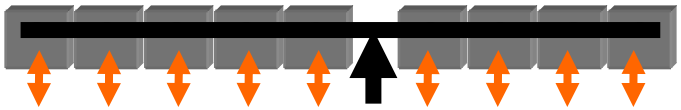
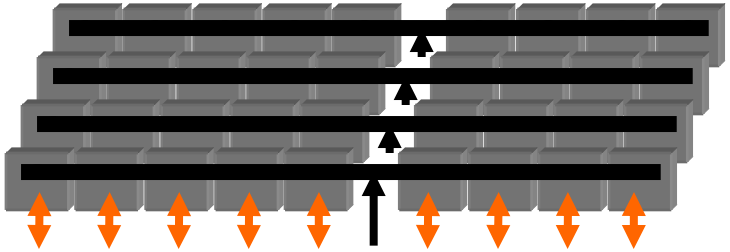
# Terminology

- ECC = Error Correction Code
- Chip Kill (also SDDC) = enhanced variant of ECC
- Rank = DRAMs sharing a select line



  - 1 rank of x8 DRAMs = 8 chips for x64 bus
    9 chips for x72 bus (ECC)
  - 1 rank of x4 DRAMs = 18 chips for x72 bus
  - 2Rx4 = 36 DRAMs
  - 4Rx4 = 72 DRAMs





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# English or Metric?

| | SDRAM | DDR1 | DDR2 & DDR3 |
|---|---|---|---|
| DIMM | 5.25 x 1.7” | 5.25 x 1.2” | 133.35 x 30mm |
| VLP | n/a | 5.25 x 0.72” | 133.35 x 18.3mm |
| SO-DIMM | 2.66 x 1.25” | 67.6 x 31.75mm | 67.6 x 30mm |

***Metric conversion finally complete…***



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# Module Configurations

| | | |
|---|---|---|
| DDR1 | Registered DIMM **(4 rank)**<br>Unbuffered DIMM<br>SO-DIMM | Micro-DIMM<br>32b-DIMM<br>**16b-SO-DIMM** |
| DDR2 | Registered DIMM **(4 rank)**<br>**Mini-RDIMM (4 rank)**<br>Unbuffered DIMM<br>**FB-DIMM** | SO-DIMM<br>Micro-DIMM<br>**16b/32b-SO-DIMM**<br>**72b-SO-RDIMM (4 rank)** |
| DDR3 | **Registered DIMM**<br>**Mini-RDIMM (4 rank)**<br>Unbuffered DIMM<br>**FB-DIMM** | SO-DIMM<br>Micro-DIMM<br>**16b/32b-SO-DIMM** |



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# DRAM Market Overview & Impact on Memory Modules



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# DRAM Density

- 1Gb transition hindered by the Perfect Storm
  - DDR1/DDR2 split on suppliers & designs
  - 110 → 90nm transition difficulties
  - 10% die penalty for 8 banks
- 512Mb DRAM will be the sweet spot through 2006!
- Implications include 2GB/slot for 2Rx4

- ➢ 4 Rank Modules will increase market share
- ➢ Stacking will be the lowest cost path to 4GB

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# Postage Stamp BGA Stack



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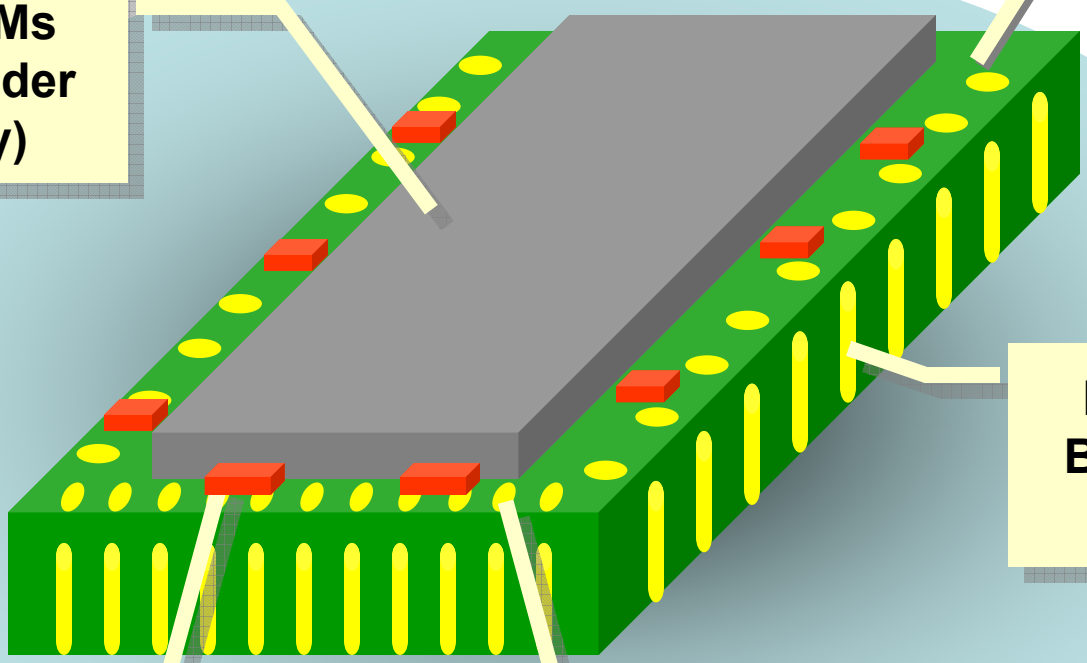
# Postage Stamp Features



2 DRAMs (one under cavity)

Cavity Substrate

High Reliability Ball-less Vertical Interconnect

Decoupling Capacitors

Probe Points on All Signals and Voltages



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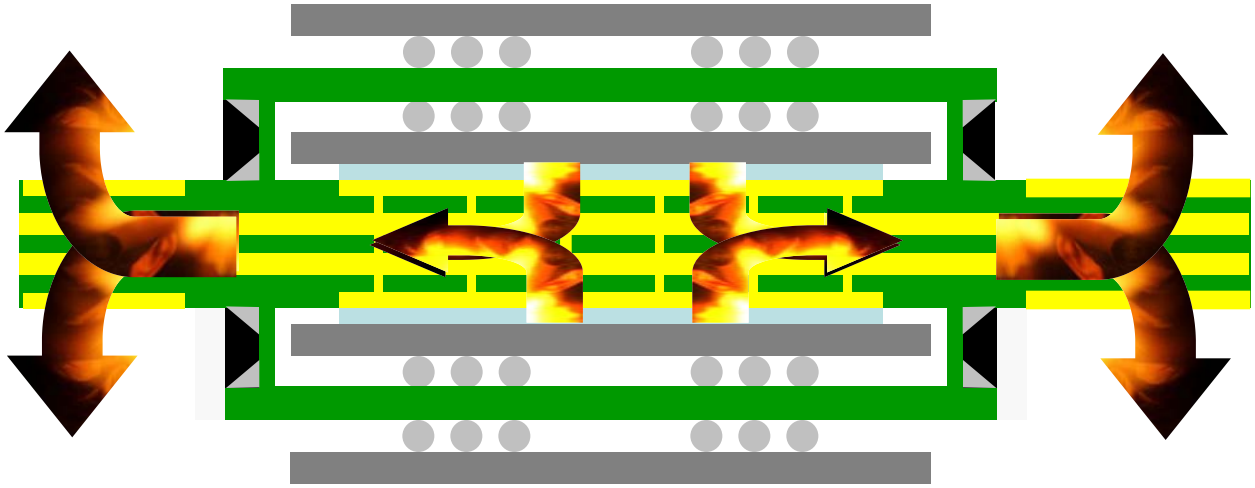
# Postage Stamp Thermal Improvements



**Thermal path to all ground planes then to surface copper flood – entire DIMM becomes a heat spreader**



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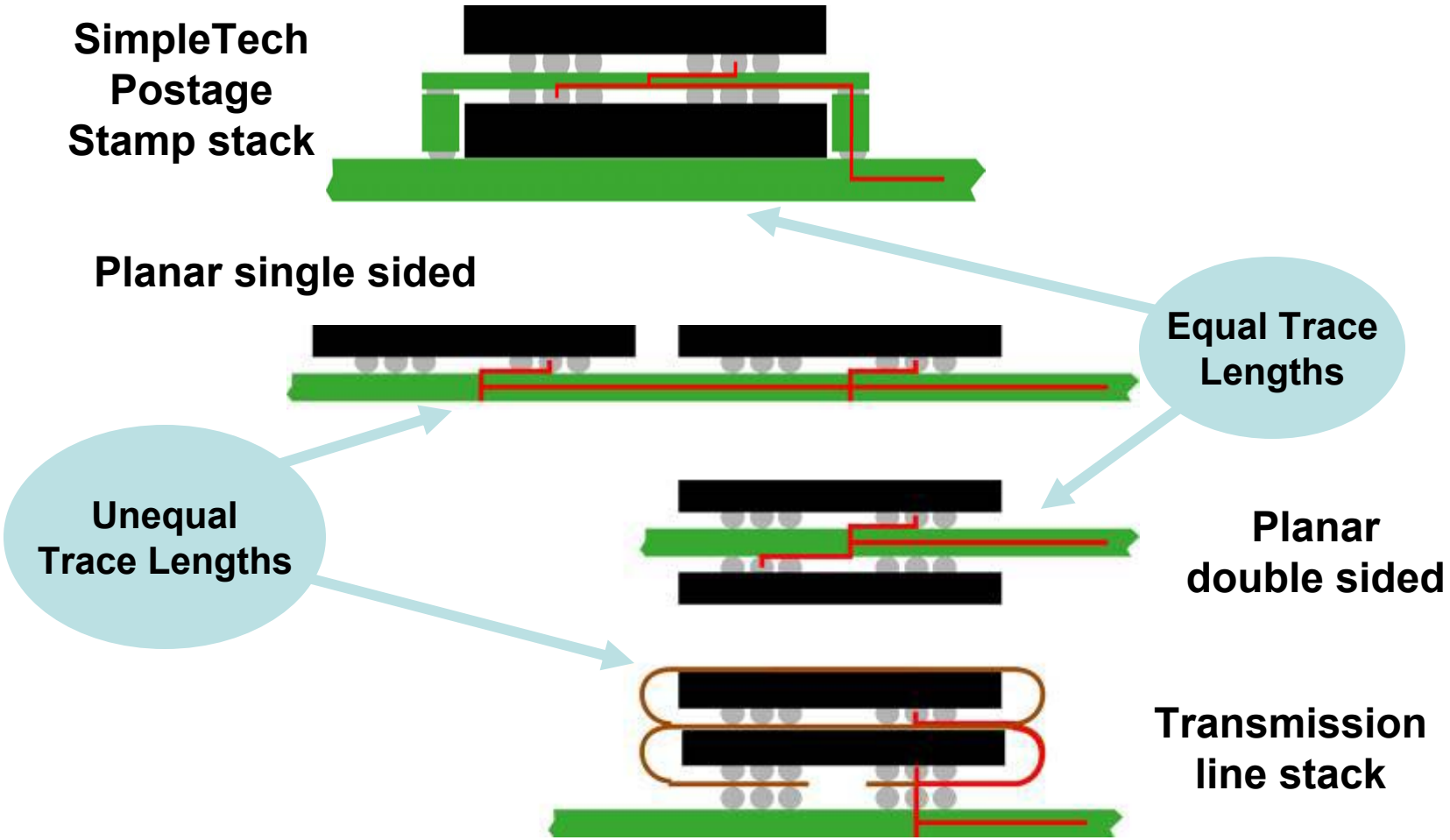
# Designing for Performance



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# Module Markets: Desktop & Mobile



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# PC Market: Unified View

| | 2005 | 2006 | 2007 |
|---|---|---|---|
| Desktop PC | DDR2-667 UDIMM<br>2 Rank | DDR2-800 UDIMM<br>2 Rank | DDR3-1066 UDIMM<br>2 Rank |
| | | | DDR3 Transition |
| Notebook PC | DDR2-667 SO-DIMM<br>2 or 4 Rank | DDR2-800 SO-DIMM<br>2 or 4 Rank | DDR3-1066 SO-DIMM<br>2 or 4 Rank |
| Subnotebook PC | DDR2-667 Micro-DIMM<br>2 or 4 Rank | DDR2-800 Micro-DIMM<br>2 or 4 Rank | DDR3-1066 Micro-DIMM<br>2 or 4 Rank |



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# Why SO- and Micro-DIMM?

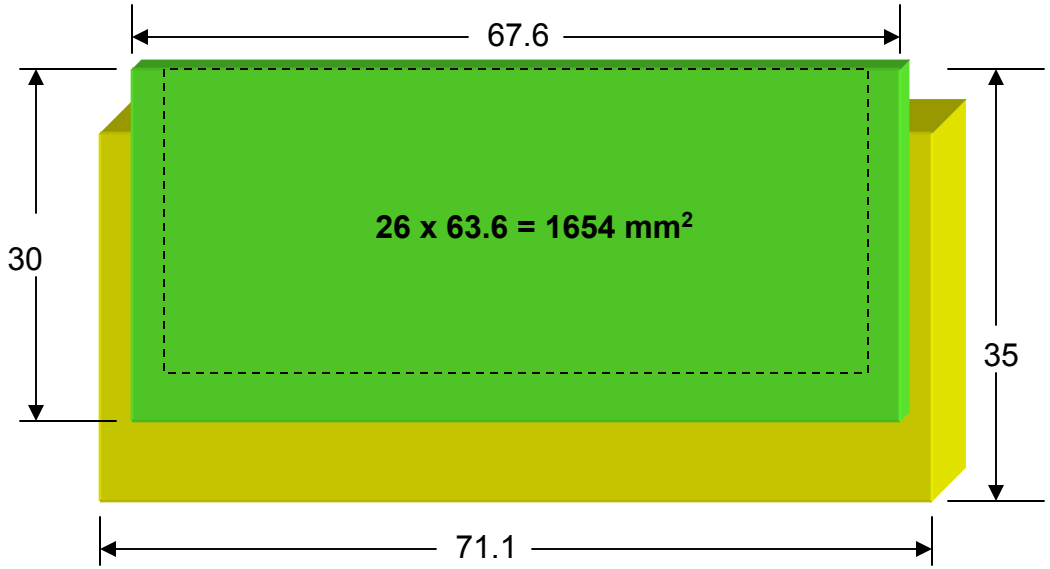
**DDR2 SO-DIMM with Edge Connector Socket**

Thickness = 5.2 mm

2D Layout efficiency =

1654 / 2489 = 66%

1GB → 79KB/mm$^3$




**142% cubic density ratio advantage using Micro-DIMM versus SO-DIMM**

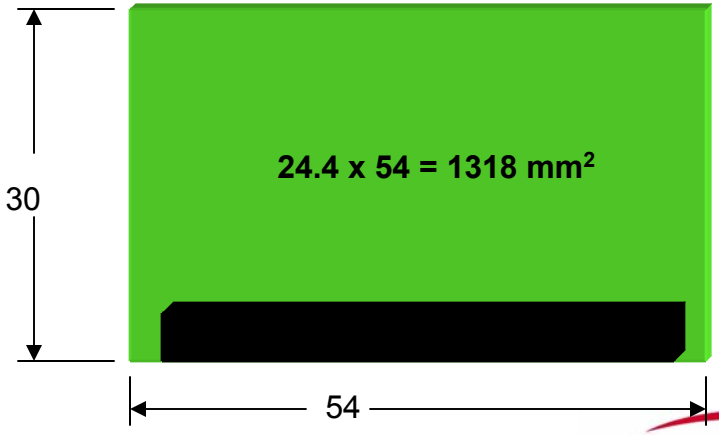
Thickness = 5.65 mm

2D Layout efficiency =

1318 / 1620 = 81%

1GB → 112KB/mm$^3$

**DDR2 Micro-DIMM with Mezzanine Connector**



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# Module Markets:
# Servers & Workstations



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# Fragmentation

Diverging views in server segment

1. RDIMM → FB-DIMM in all segments;
   DDR2 FB-DIMM a huge success

2. DDR2 → DDR3 RDIMM;
   FB-DIMM not “real” until DDR3 if at all

JEDEC roadmaps support either path



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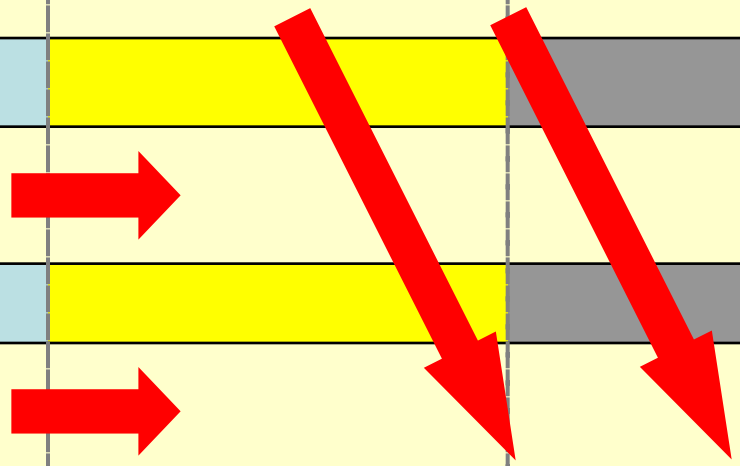
# Server Market View #1

| | 2005 | 2006 | 2007 | |
|---|---|---|---|---|
| HE Server | DDR2-400 RDIMM 2 Rank | DDR2-533 FB-DIMM | DDR2-667 FB-DIMM | DDR3-800 FB-DIMM |
| Mid Server | DDR2-400 RDIMM 2 Rank | | | |
| LE Server | DDR2-400 RDIMM 2 Rank | | | |
| HPC | DDR2-533 UDIMM 2 Rank | DDR2-667 UDIMM 2 Rank | DDR3-1333 UDIMM 2 Rank | |



"RDIMM is obsolete next year"



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# Server Market View #2

| | 2005 | 2006 | 2007 |
|---|---|---|---|
| HE Server | DDR1-266 RDIMM 4 Rank | DDR2-533 RDIMM 4 Rank | FB-DIMM in 2008? |
| Mid Server | DDR1-333 RDIMM 4 Rank | DDR2-667 RDIMM 4 Rank | DDR3-1333 RDIMM 4 Rank |
| LE Server | DDR1-400 RDIMM 4 Rank | DDR2-667 RDIMM 4 Rank | DDR3-1333 RDIMM 4 Rank |
| HPC | DDR1-400 UDIMM 2 Rank | DDR2-667 UDIMM 2 Rank | DDR3-1333 UDIMM 2 Rank |



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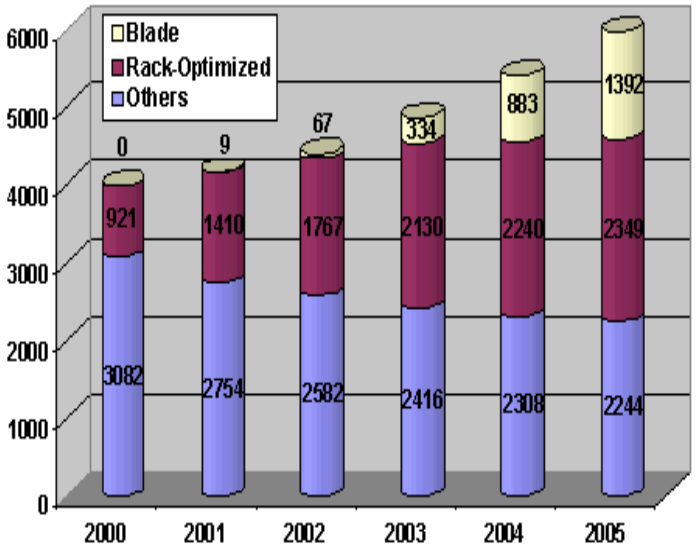
# Form Factor Wars

- 1.2” (30mm) standard chosen in 1999 based on 1U server market projections

HP First to Reach Milestone of 100,000 Blade Servers Sold

- But, market fragmenting
  - Blade needs 18.3mm (VLP)
  - 1U needs 30mm (LP)
  - 2U can use 38mm or taller




- OEMs “demand” one size fits all … but …



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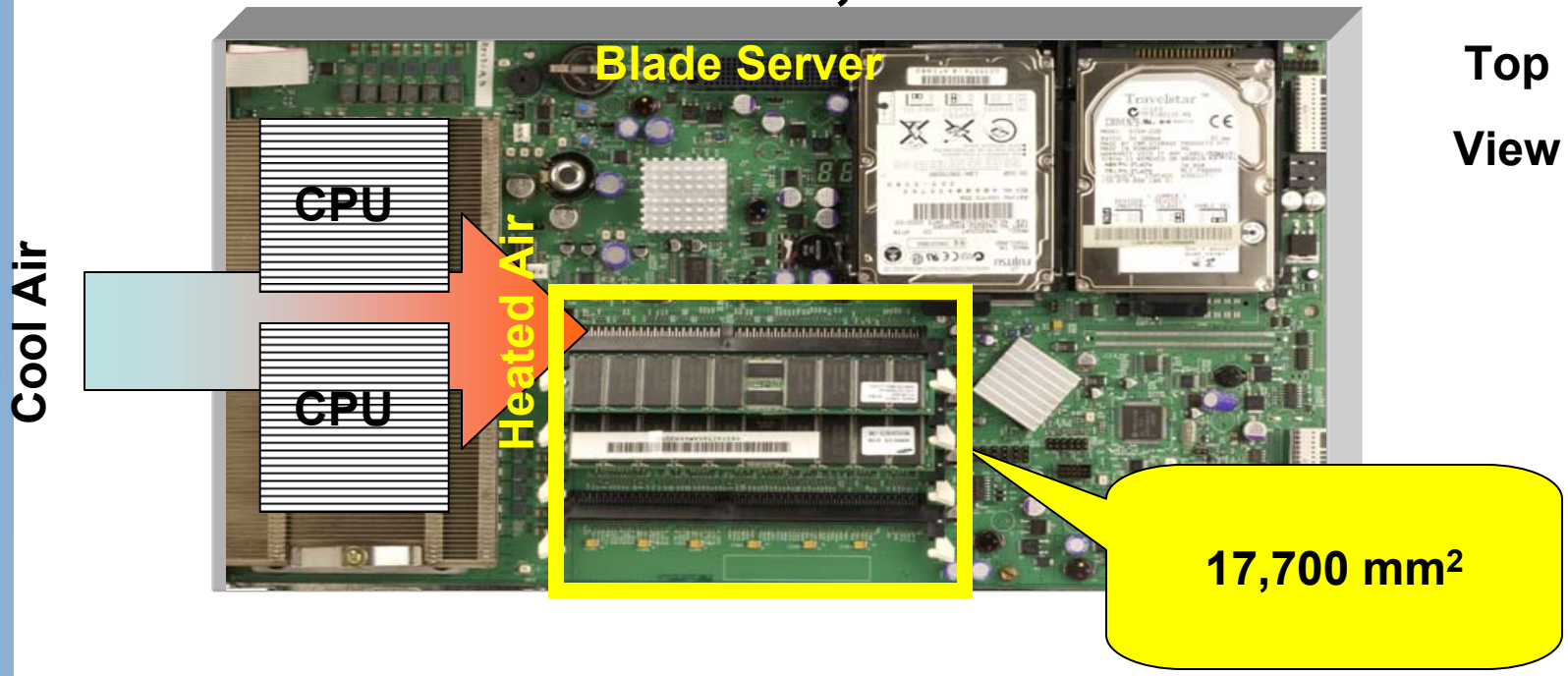
# Blade Server, 1.2” Module



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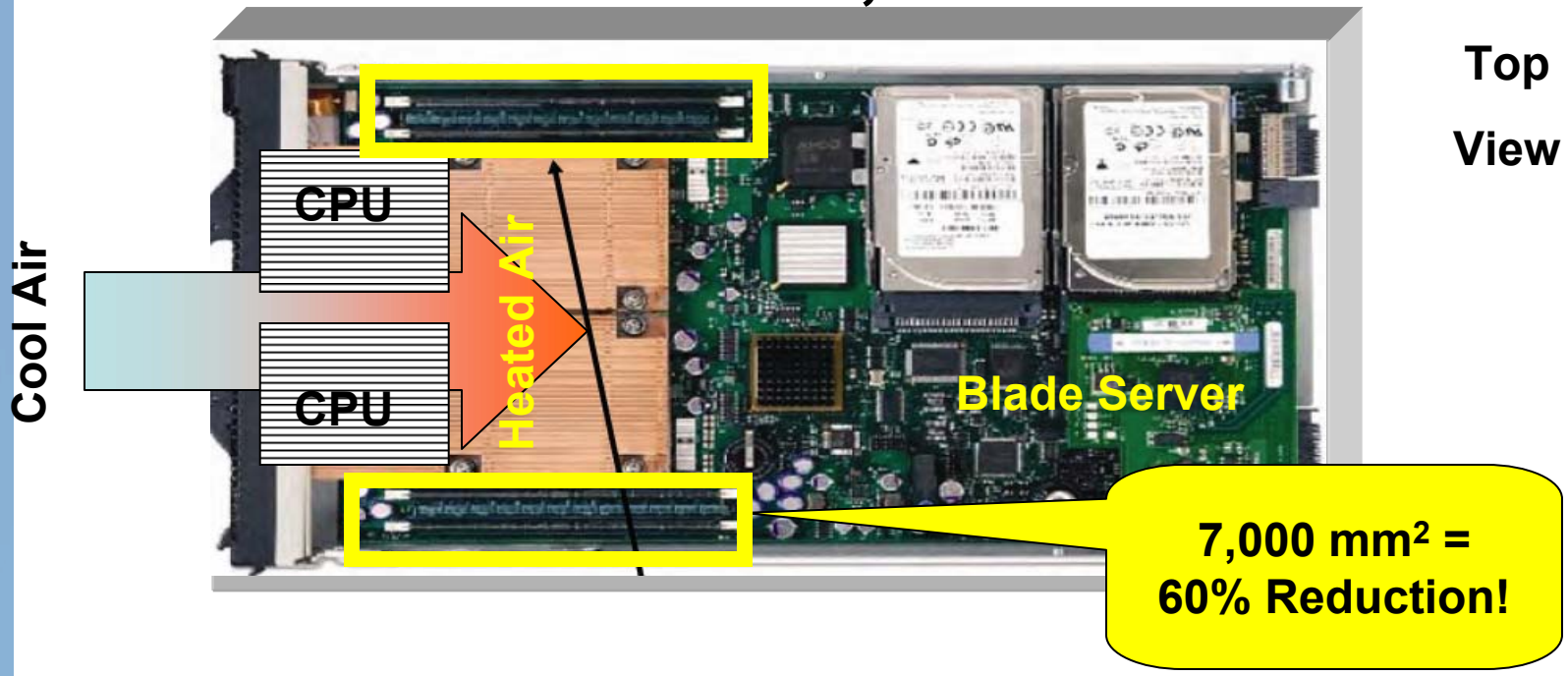
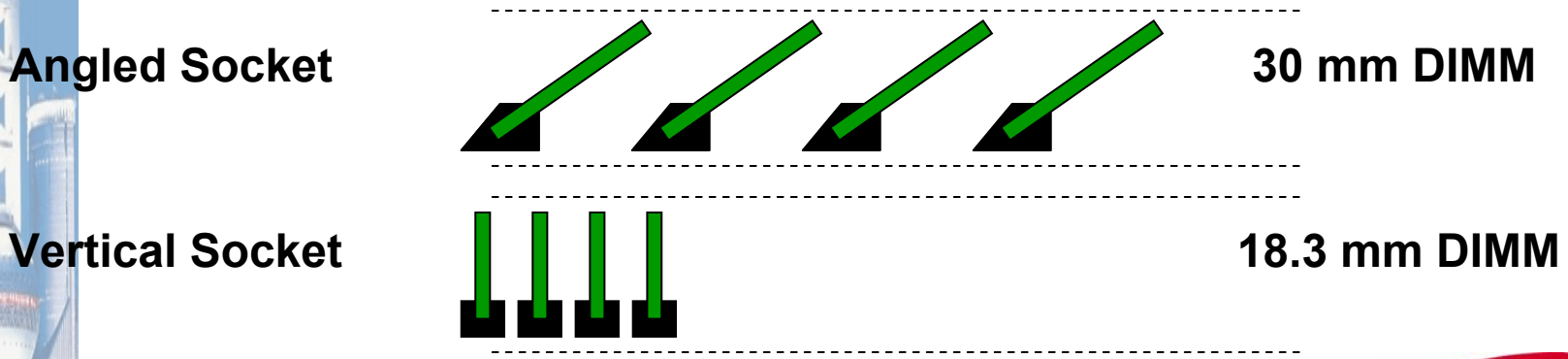
# Blade Server, VLP DIMM



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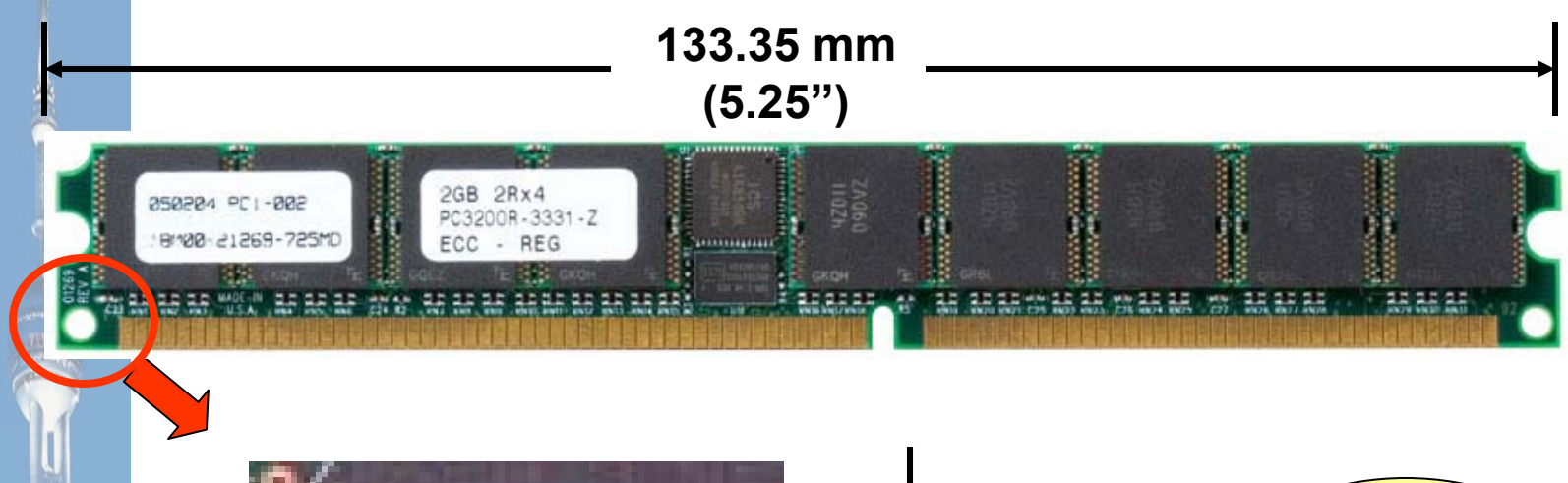
# The VLP Form Factor





4 mm
(0.158”)

14.3 mm
(0.56”)
Usable
Layout Area



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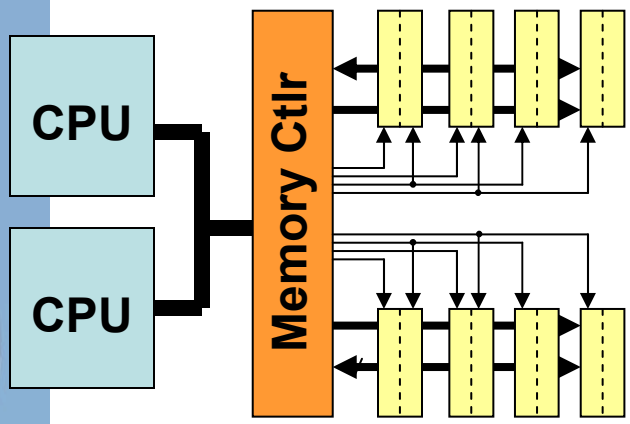
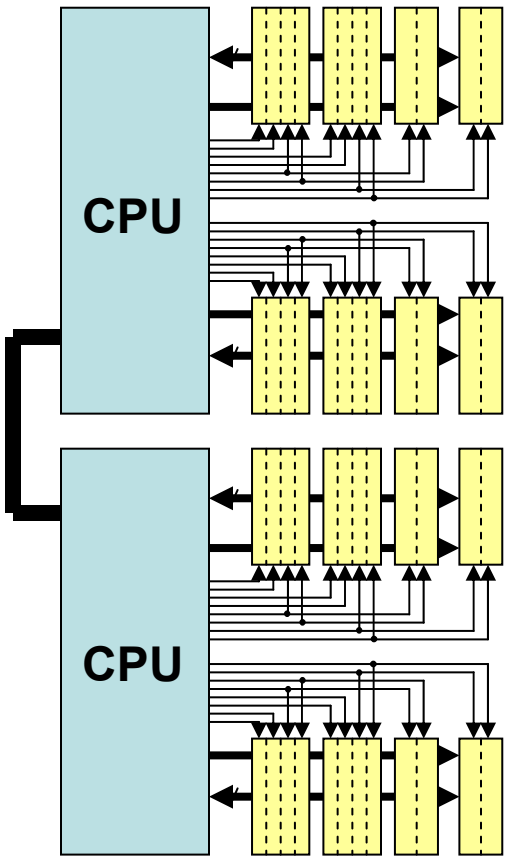
# 4 Rank RDIMM




← From 8 ranks (16GB) max for dual CPU…

… to 32 ranks (64GB) max for dual CPU →




Requires 2 extra rank select signals routed on motherboard

BIOS updated to detect SPD byte 5 = ‘4’

DDR1 & DDR2 4 rank specs approved



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# Fully Buffered DIMM



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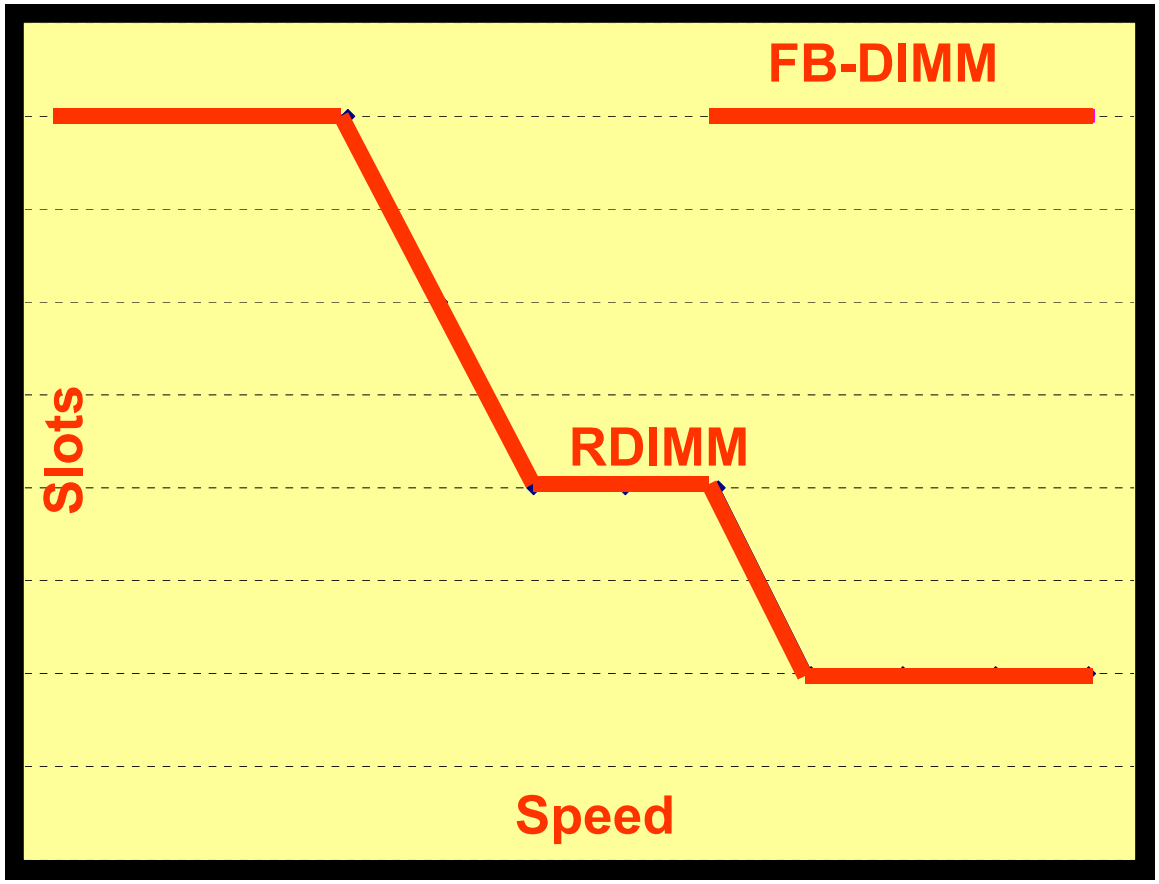
# Motivation for FB-DIMM




**FB-DIMM supports 8 slots per channel at any speed**

**As speeds increase, the number of RDIMMs per channel decrease**



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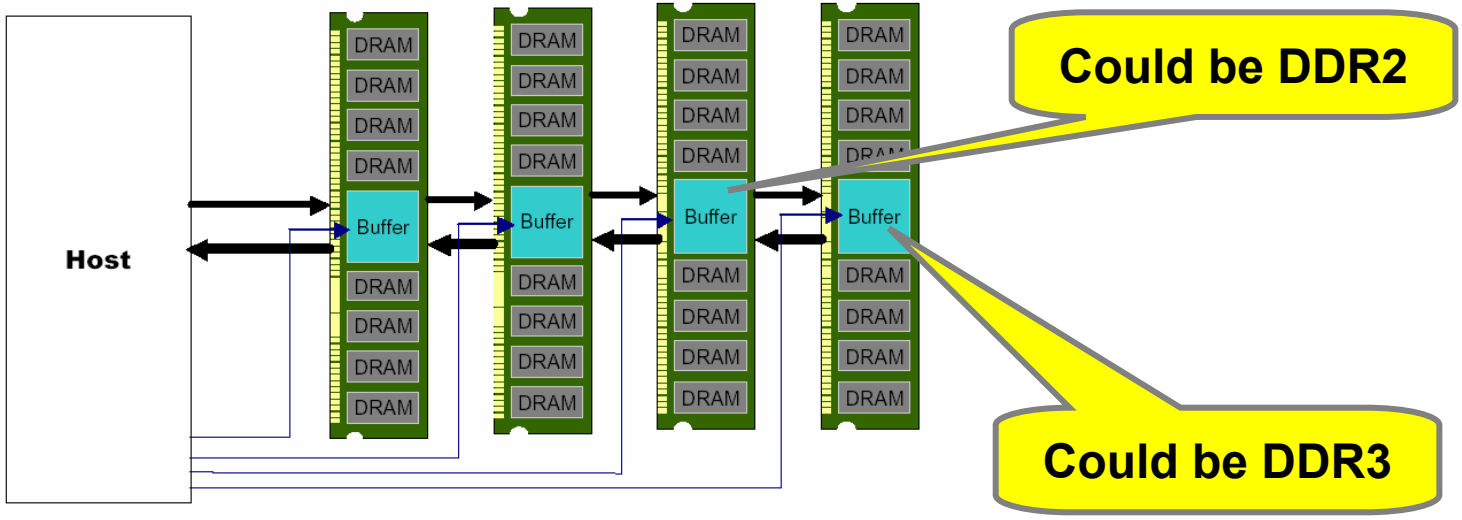
# Fully Buffered DIMM




☺ Solves stub bus timing challenges

☺ 16GB per channel (8 DIMMs per channel)

☺ Eases DDR2 → DDR3 transition

☹ Cost and thermal issues may limit use

☹ Single DIMM failure can cause channel failure

☹ Intellectual property questions delay approval



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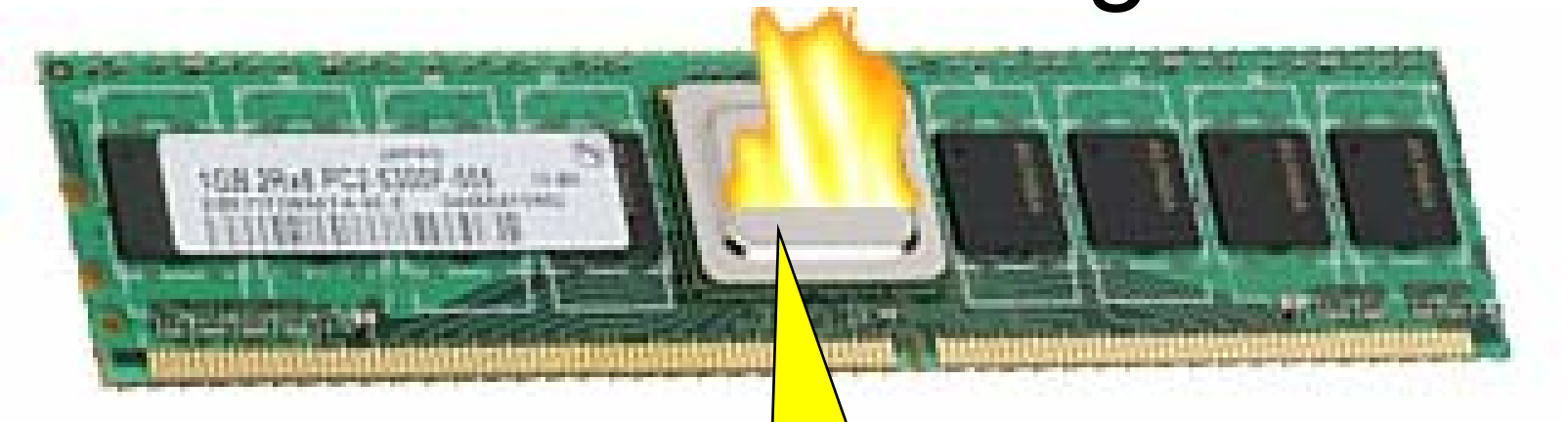
# FB-DIMM Design



**4.8GHz → 9.6GHz**

**5-7W of power**

**Center of module – no good direction for cooling**

**Constantly draining power through termination**

**Expensive 655 ball BGA package**

**Requires heat sink**

**Very tricky thermal design challenge**



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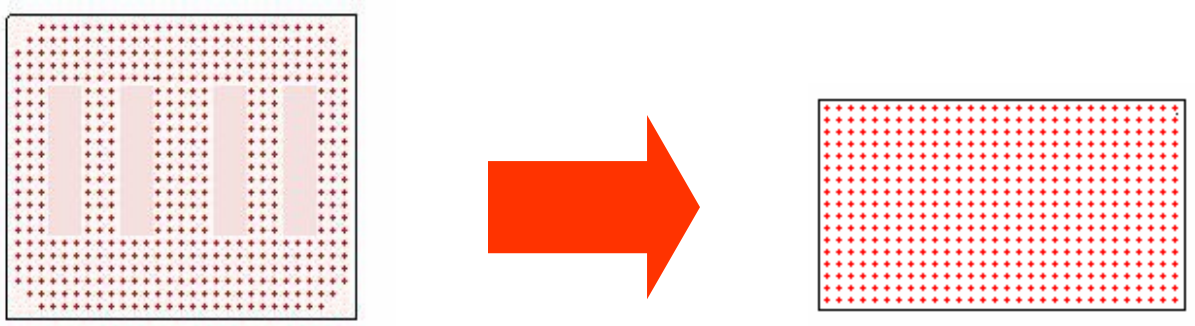
# Under Consideration



- VLP FB-DIMM
  - Repackaging the AMB to 14mm for VLP
- 4 Rank support
  - 4GB per slot → 8GB per slot
- Spare bit lane
  - Increased reliability for non-stop mission critical systems



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# Unbuffered & Registered DIMMs



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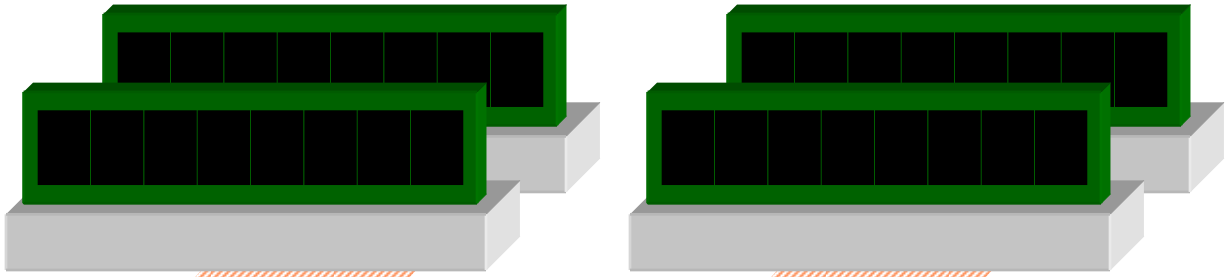
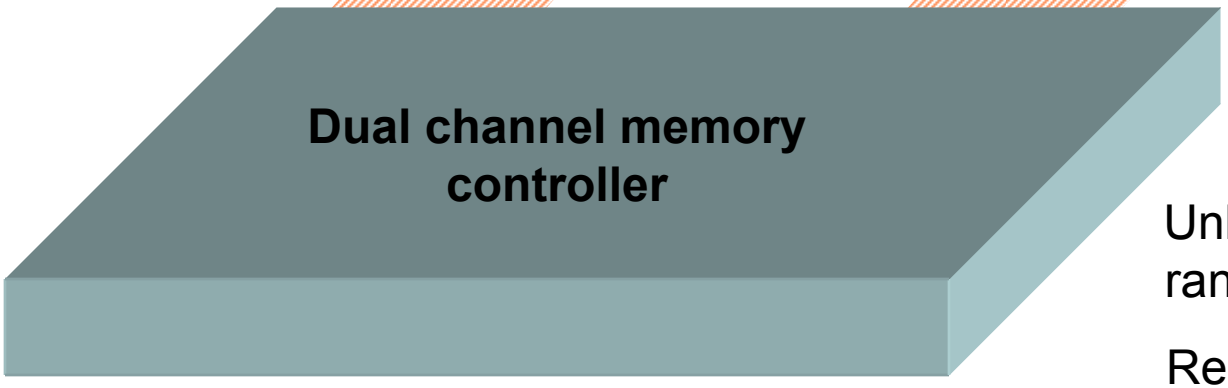
# Typical System Configuration

Two slots per channel






Unbuffered: 2 ranks per slot — 8GB

Registered: 4 ranks per slot — 16GB



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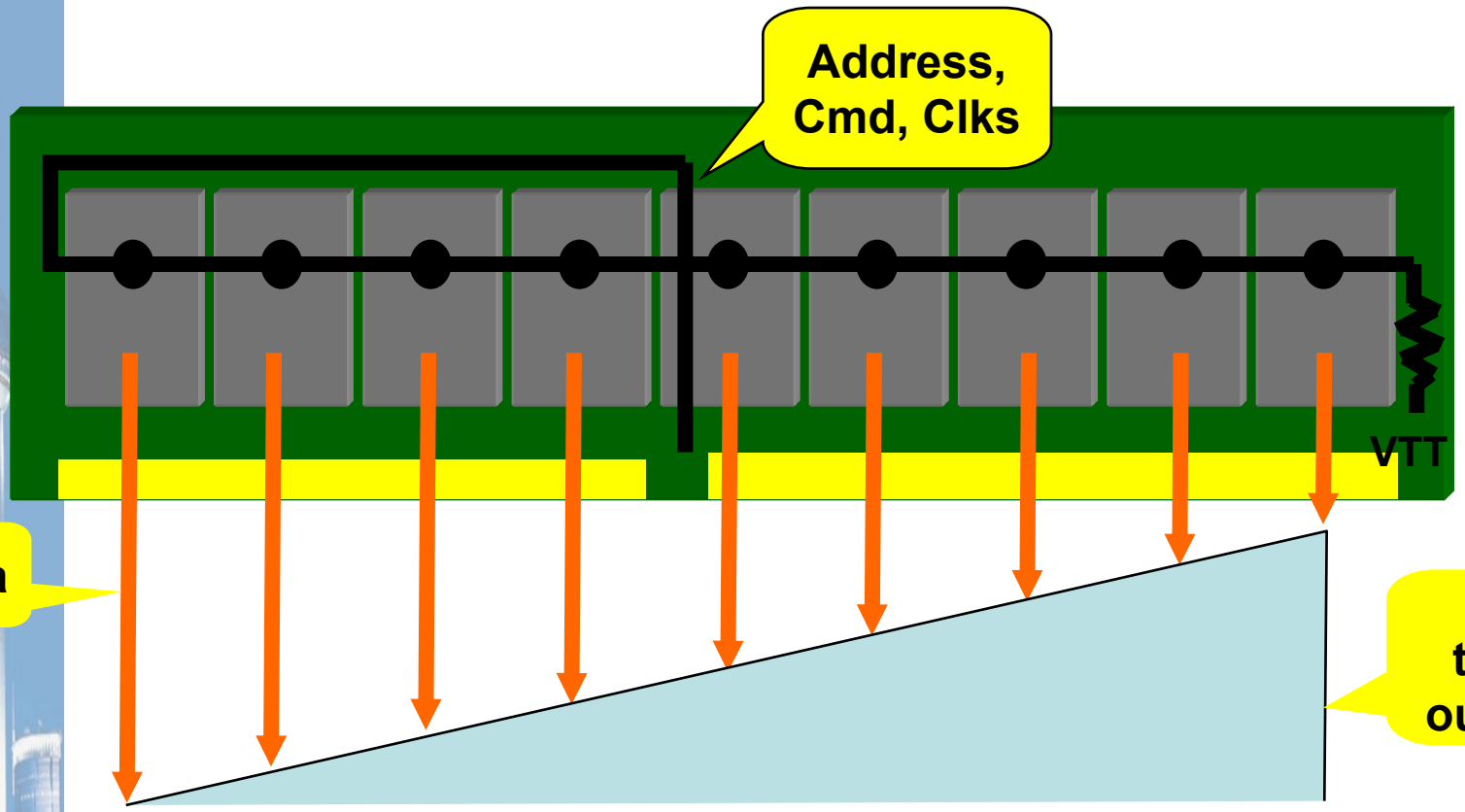
# DDR3 Unbuffered Modules




**VLP Form Factor Impractical!!!**



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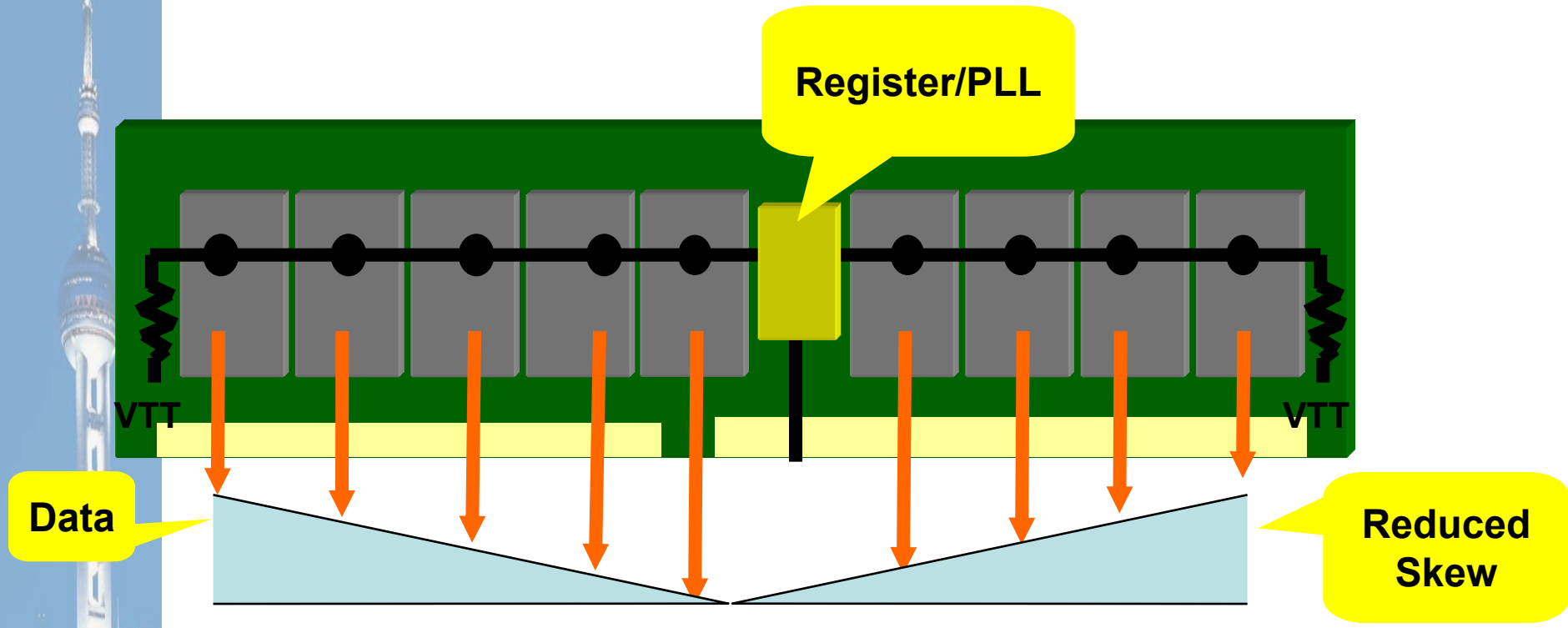
# DDR3 RDIMM Fly-By




**Support for 2 ranks (36 DRAMs)**
**and 4 ranks (72 DRAMs) – VLP enabled**



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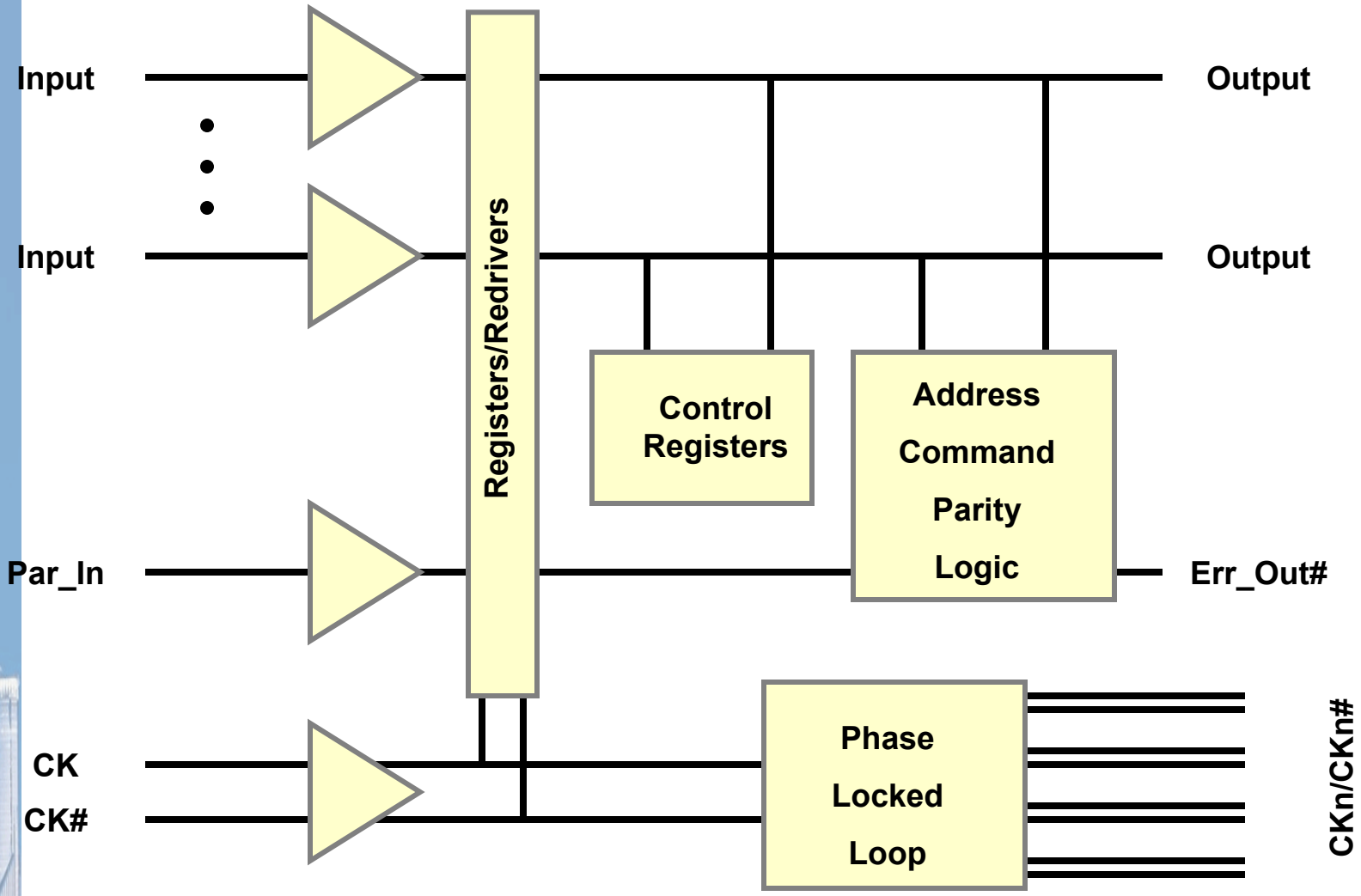
# Registering Clock Driver



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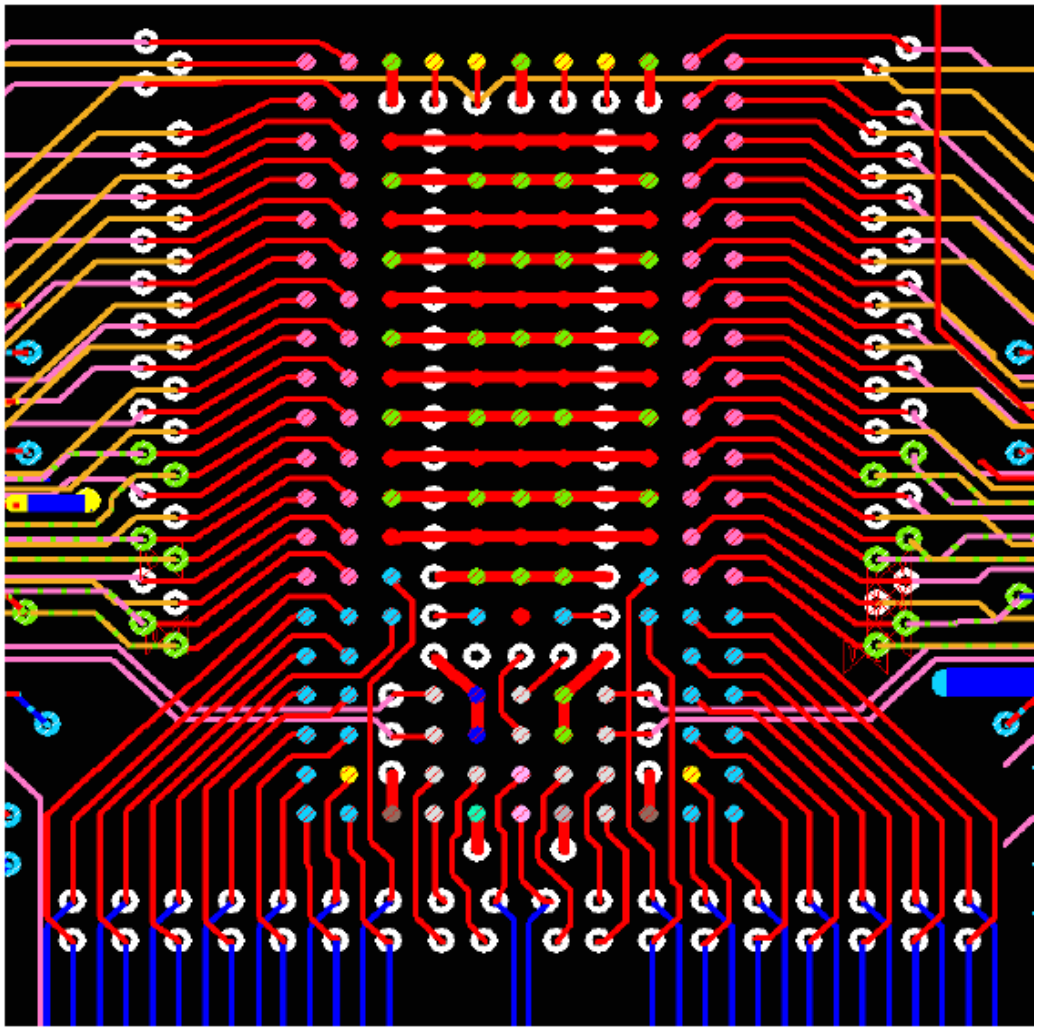
# DDR3 RDIMM

Register/PLL ballout defined for clean routing





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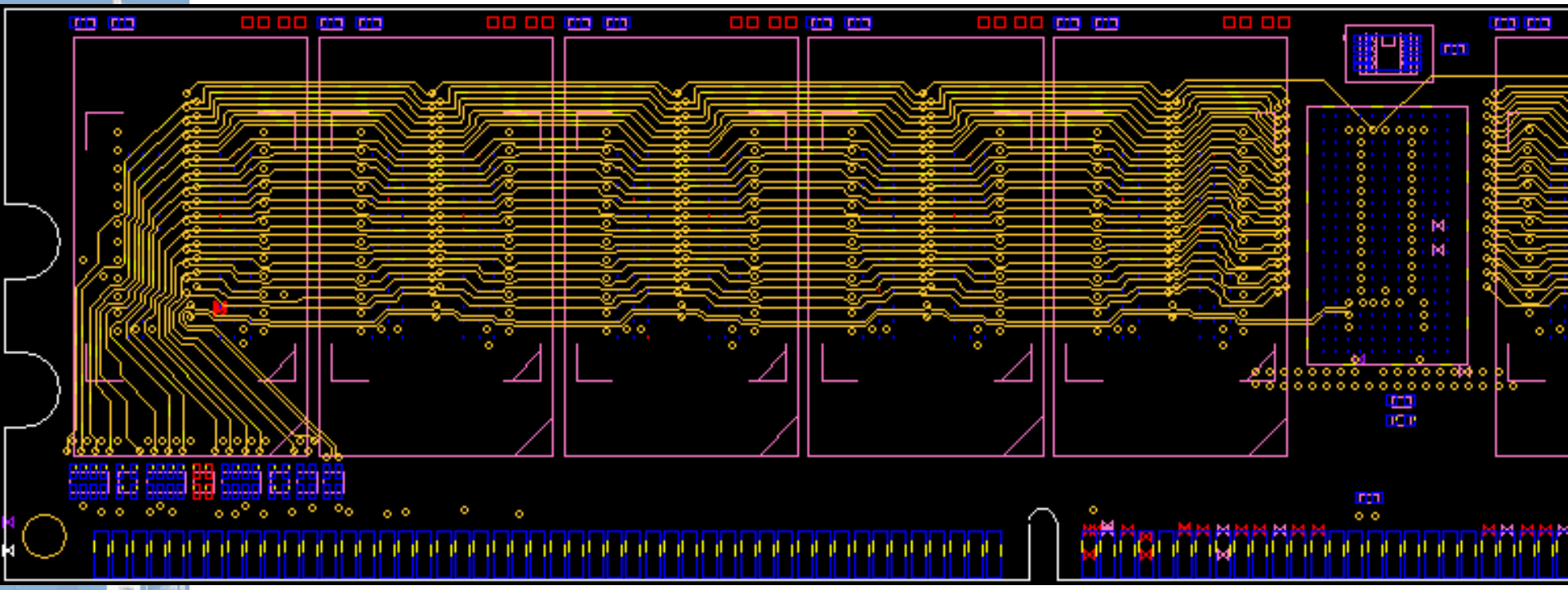
# Address Bus Routing



*So clean it's beautiful!*



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# DDR3 RDIMM Summary

- Compatible with UDIMM controller
  - Eases adoption for existing controllers
- Single low pin count register/PLL
  - Lower cost
  - Simpler layout
  - Size enables VLP (18.3mm) RDIMM
- Integrated PLL with only 4 output pairs
  - Lower power
- 4 rank support designed in



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# Industry Wide Support

| | |
|---|---|
| **Raw card A: 1Rx8 (1-4 GB)** | **Micron** |
| **Raw card B: 2Rx8 (2-8 GB)** | **Samsung** |
| **Raw card C: 1Rx4 (2-8 GB)** | **Elpida** |
| **Raw card D: 2Rx4 (4-16 GB) – Stacked** | **SimpleTech** |
| **Raw card E: 2Rx4 (4-16 GB) – Planar** | **Infineon** |



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# What Happens in Server & Workstation Market?



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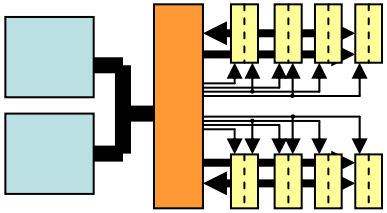
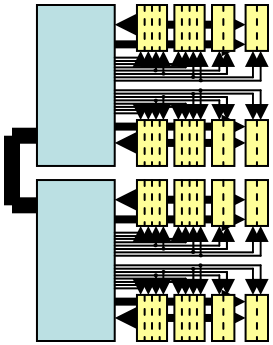
# FB-DIMM or RDIMM?





8 DIMM channel
X 2GB IMM
= 16GB hannel

- Low ount
- High
- High

Bigg tal

**Too early to determine which will be the next mainstream server memory.**



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# Router/Networking Markets



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# Router & Networking

| | 2005 | 2006 | 2007 |
|---|---|---|---|
| High End Routers | DDR1 RDIMM | DDR2 Mini-RDIMM | DDR3 Mini-RDIMM |
| | 72b-SO-RDIMM (4 rank) | | |
| Low End Routers | DDR1 SO-DIMM | DDR2 SO-DIMM | DDR3 SO-DIMM |

- Split between those that need ECC and those that don't need ECC
- FB-DIMM not a fit for this market



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# Mini-RDIMM Form Factor

**82mm versus 133mm = 40% reduction in size versus full size RDIMM**

- JEDEC ballot in process to add:
  - Support for address/command parity
  - Support for 4 ranks of memory
- Task group for DDR3 Mini-RDIMM



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# New! 72b-SO-RDIMM


- SO-DIMM sized module with 72 bit bus
- Reuse existing mobile sockets (right angle) with no voltage key change
- Performance to DDR2-667
- 512MB/1GB sweet spot, 2GB capable



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# 72b-SO-RDIMM Pinout

| Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 2 | $V_{SS}$ | 51 | DQ18 | 52 | $V_{SS}$ | 101 | $V_{DD}$ | 102 | A3 | 151 | $V_{SS}$ | 152 | $V_{SS}$ |
| 3 | DQ0 | 4 | DQ4 | 53 | DQ19 | 54 | DQ28 | 103 | A5 | 104 | A1 | 153 | $\overline{DQS5}$ | 154 | DM5 |
| 5 | $V_{SS}$ | 6 | DQ5 | 55 | $V_{SS}$ | 56 | DQ29 | 105 | A4 | 106 | $V_{DD}$ | 155 | DQS5 | 156 | $V_{SS}$ |
| 7 | DQ1 | 8 | $V_{SS}$ | 57 | DQ24 | 58 | $V_{SS}$ | 107 | A2 | 108 | A0 | 157 | $V_{SS}$ | 158 | DQ46 |
| 9 | $\overline{DQS0}$ | 10 | DM0 | 59 | DQ25 | 60 | DM3 | 109 | $V_{DD}$ | 110 | BA1 | 159 | DQ42 | 160 | DQ47 |
| 11 | DQS0 | 12 | $V_{SS}$ | 61 | $V_{SS}$ | 62 | $V_{SS}$ | 111 | A10 / AP | 112 | $\overline{RAS}$ | 161 | DQ43 | 162 | $V_{SS}$ |
| 13 | $V_{SS}$ | 14 | DQ6 | 63 | $\overline{DQS3}$ | 64 | DQ30 | 113 | BA0 | 114 | $V_{DD}$ | 163 | $V_{SS}$ | 164 | DQ52 |
| 15 | DQ2 | 16 | DQ7 | 65 | DQS3 | 66 | DQ31 | 115 | $\overline{WE}$ | 116 | $\overline{S0}$ | 165 | DQ48 | 166 | DQ53 |
| 17 | DQ3 | 18 | $V_{SS}$ | 67 | $V_{SS}$ | 68 | $V_{SS}$ | 117 | $V_{DD}$ | 118 | ODT | 167 | DQ49 | 168 | $V_{SS}$ |
| 19 | $V_{SS}$ | 20 | DQ12 | 69 | DQ26 | 70 | CB4 | 119 | $\overline{CAS}$ | 120 | $V_{DD}$ | 169 | $V_{SS}$ | 170 | DM6 |
| 21 | DQ8 | 22 | DQ13 | 71 | DQ27 | 72 | CB5 | 121 | $\overline{S1}$ | 122 | A13 | 171 | $\overline{DQS6}$ | 172 | $V_{SS}$ |
| 23 | DQ9 | 24 | $V_{SS}$ | 73 | $V_{SS}$ | 74 | $V_{SS}$ | 123 | $V_{DD}$ | 124 | $V_{SS}$ | 173 | DQS6 | 174 | DQ54 |
| 25 | $V_{SS}$ | 26 | DM1 | 75 | CB0 | 76 | DM8 | 125 | NC/ $\overline{S3}$ | 126 | CK | 175 | $V_{SS}$ | 176 | DQ55 |
| 27 | $\overline{DQS1}$ | 28 | $V_{SS}$ | 77 | CB1 | 78 | $V_{SS}$ | 127 | $V_{SS}$ | 128 | $\overline{CK}$ | 177 | DQ50 | 178 | $V_{SS}$ |
| 29 | DQS1 | 30 | DQ14 | 79 | $V_{SS}$ | 80 | CB6 | 129 | DQ32 | 130 | $V_{SS}$ | 179 | DQ51 | 180 | DQ60 |
| 31 | $V_{SS}$ | 32 | DQ15 | 81 | $\overline{DQS8}$ | 82 | CB7 | 131 | DQ33 | 132 | DQ36 | 181 | $V_{SS}$ | 182 | DQ61 |
| 33 | DQ10 | 34 | $V_{SS}$ | 83 | DQS8 | 84 | $V_{SS}$ | 133 | $V_{SS}$ | 134 | DQ37 | 183 | DQ56 | 184 | $V_{SS}$ |
| 35 | DQ11 | 36 | DQ20 | 85 | $V_{SS}$ | 86 | CB2 | 135 | $\overline{DQS4}$ | 136 | $V_{SS}$ | 185 | DQ57 | 186 | DM7 |
| 37 | $V_{SS}$ | 38 | DQ21 | 87 | CKE | 88 | CB3 | 137 | DQS4 | 138 | DM4 | 187 | $V_{SS}$ | 188 | DQ62 |
| 39 | DQ16 | 40 | $V_{SS}$ | 89 | NC/ $\overline{S2}$ | 90 | $V_{SS}$ | 139 | $V_{SS}$ | 140 | $V_{SS}$ | 189 | $\overline{DQS7}$ | 190 | $V_{SS}$ |
| 41 | DQ17 | 42 | $\overline{RESET}$ | 91 | NC/ A14 | 92 | A12 | 141 | DQ34 | 142 | DQ38 | 191 | DQS7 | 192 | DQ63 |
| 43 | $V_{SS}$ | 44 | DM2 | 93 | $V_{DD}$ | 94 | A9 | 143 | DQ35 | 144 | DQ39 | 193 | DQ58 | 194 | SDA |
| 45 | $\overline{DQS2}$ | 46 | $V_{SS}$ | 95 | BA2 | 96 | A8 | 145 | $V_{SS}$ | 146 | $V_{SS}$ | 195 | $V_{SS}$ | 196 | SCL |
| 47 | DQS2 | 48 | DQ22 | 97 | A11 | 98 | $V_{DD}$ | 147 | DQ40 | 148 | DQ44 | 197 | DQ59 | 198 | SA1 |
| 49 | $V_{SS}$ | 50 | DQ23 | 99 | A7 | 100 | A6 | 149 | DQ41 | 150 | DQ45 | 199 | $V_{DD}$SPD | 200 | SA0 |

**Not pin compatible with 64bit SO-DIMM, but no damage occurs on accidental mismatch**



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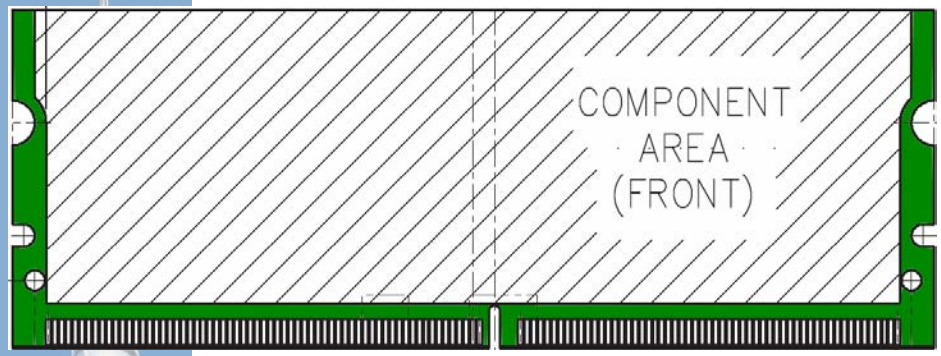
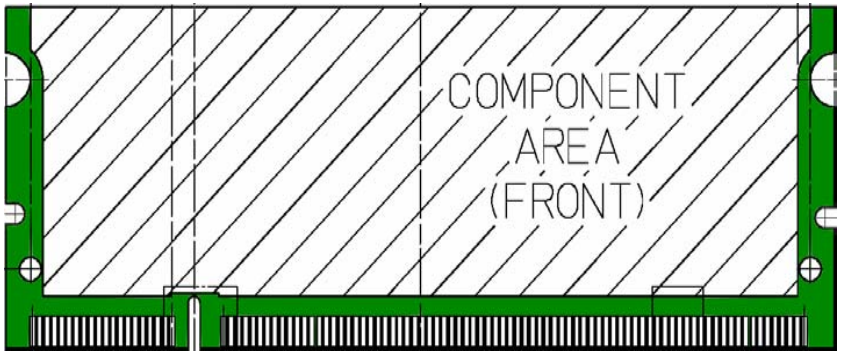
# Mini-RDIMM vs 72b-SO-RDIMM




- Module = 82 x 30mm
- Component area = 78 x 26mm
- 244 pins, 0.6 mm pitch

- Module = 67.6 x 30mm
- Component area = 63.6 x 26mm
- 200 pins, 0.6 mm pitch



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# Key Differences

| Mini-RDIMM | 72b-SO-RDIMM |
| --- | --- |
| • X4 DRAM supported<br>• 4 rank supported (proposed)<br>• 8GB max<br>• 3 clock pairs → unbuffered supported<br>• Address/command parity supported (proposed) | • X4 DRAM not supported<br>• 4 rank supported<br>• 4GB max<br>• One clock pair → PLL needed<br>• Address/command parity not possible (no pins) |



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# Peripheral Markets



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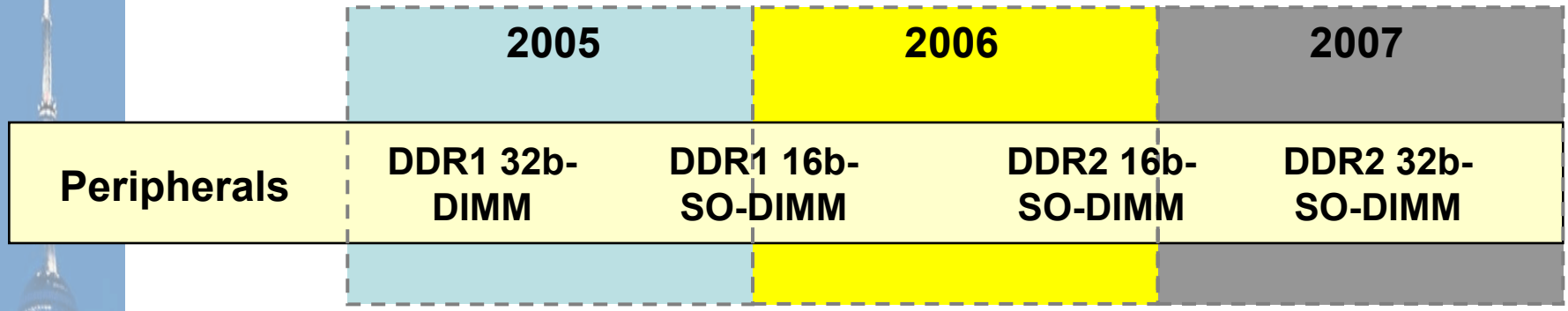
# Peripherals




- Devices that need smaller granularity
  - A single 512Mb chip contains 64MB of data!
- Small footprint is desirable
  - 1 to 4 DRAMs typical
- Reuses SDRAM 144-pin SO-DIMM form
- Common pinout for DDR1/2/3 and 16/32 bits



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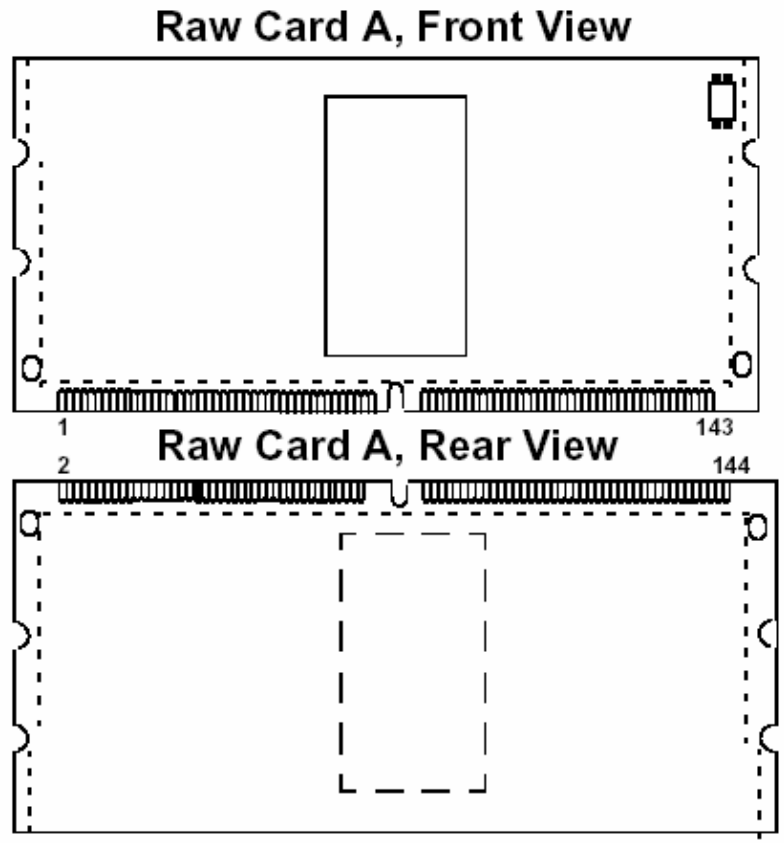
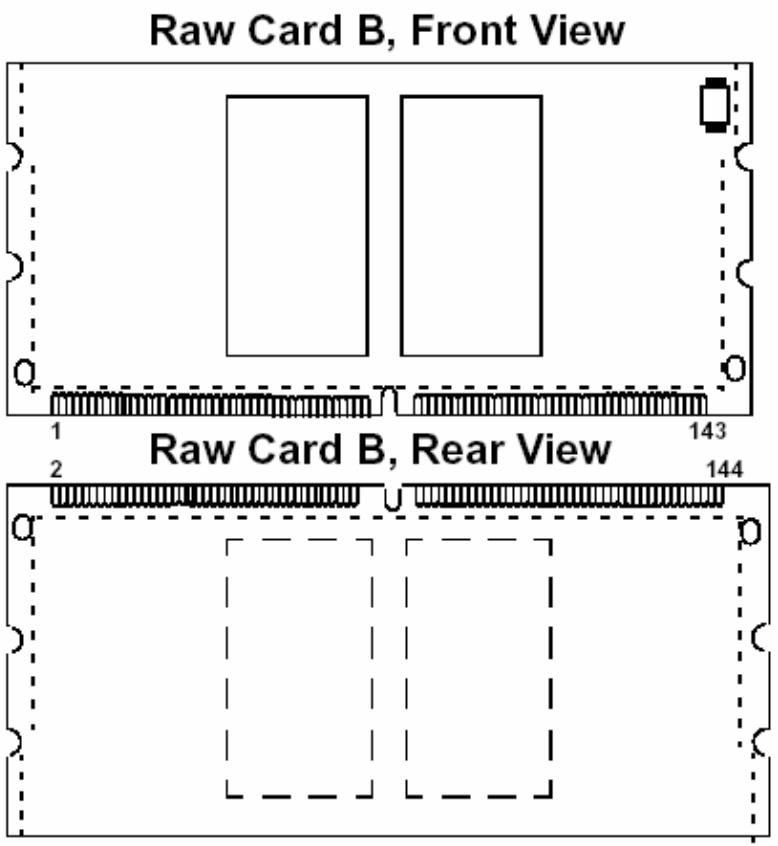
# Modules for Peripherals



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# Memory Module Summary

- DDR2 transition under way, DDR3 coming
- PC market form factors fairly stable
  - UDIMM, SO-DIMM, Micro-DIMM
  - DDR1 → DDR2 → DDR3
- Server market fragmenting
  - RDIMM → FB-DIMM or RDIMM → RDIMM?
  - Module height = 30mm? 18.3mm?
- Networking: Mini-RDIMM **72b-SO-RDIMM (4 rank)**
- Peripherals: 16b-SO-DIMM



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# Thank You

Questions?



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